

NBWAA

Low Cost Los Angeles 10L

LA-5821P REV 1.0 Schematics

Intel Penryn/ Cantiga/ ICH9M

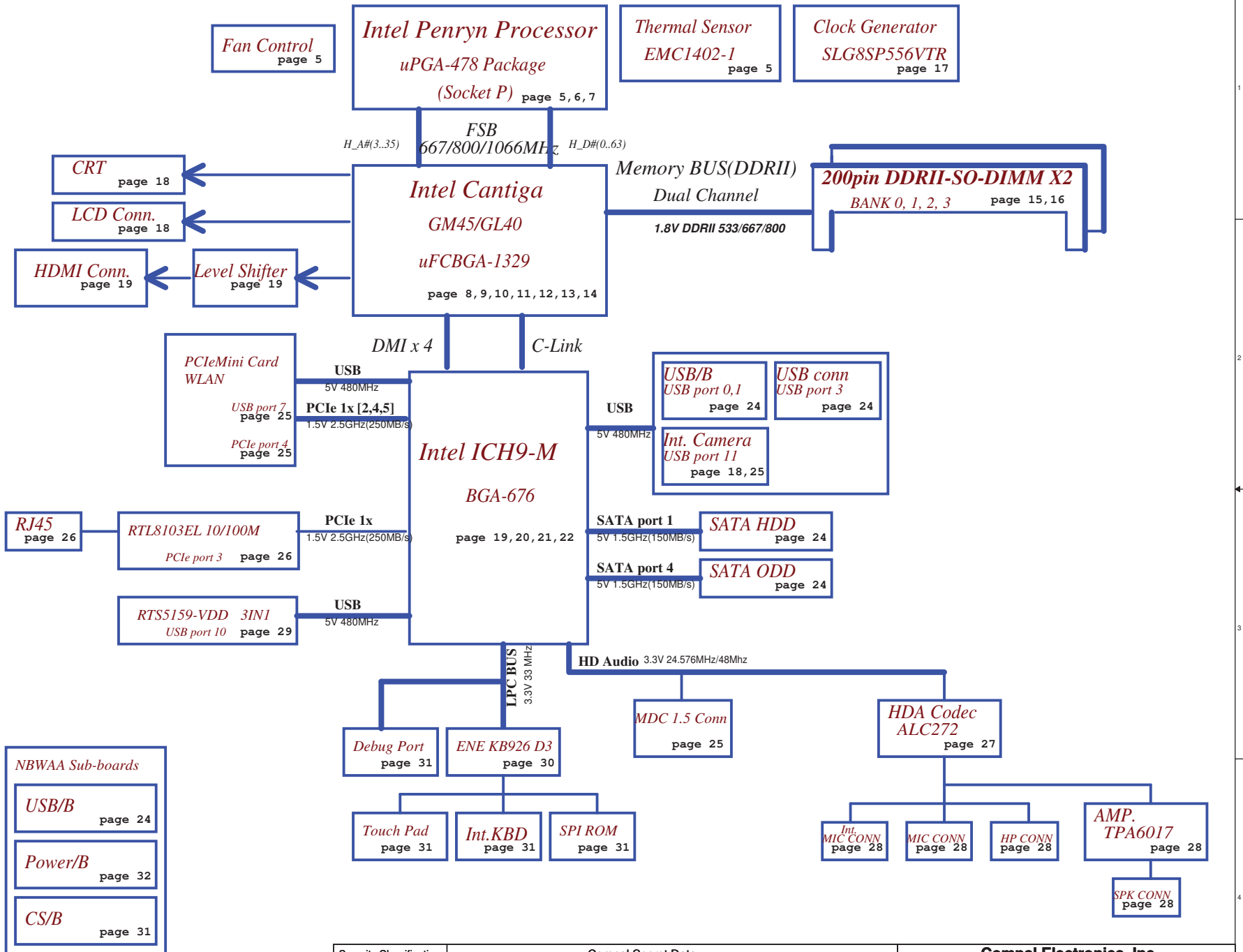
2008-08-10 Rev. 1.0

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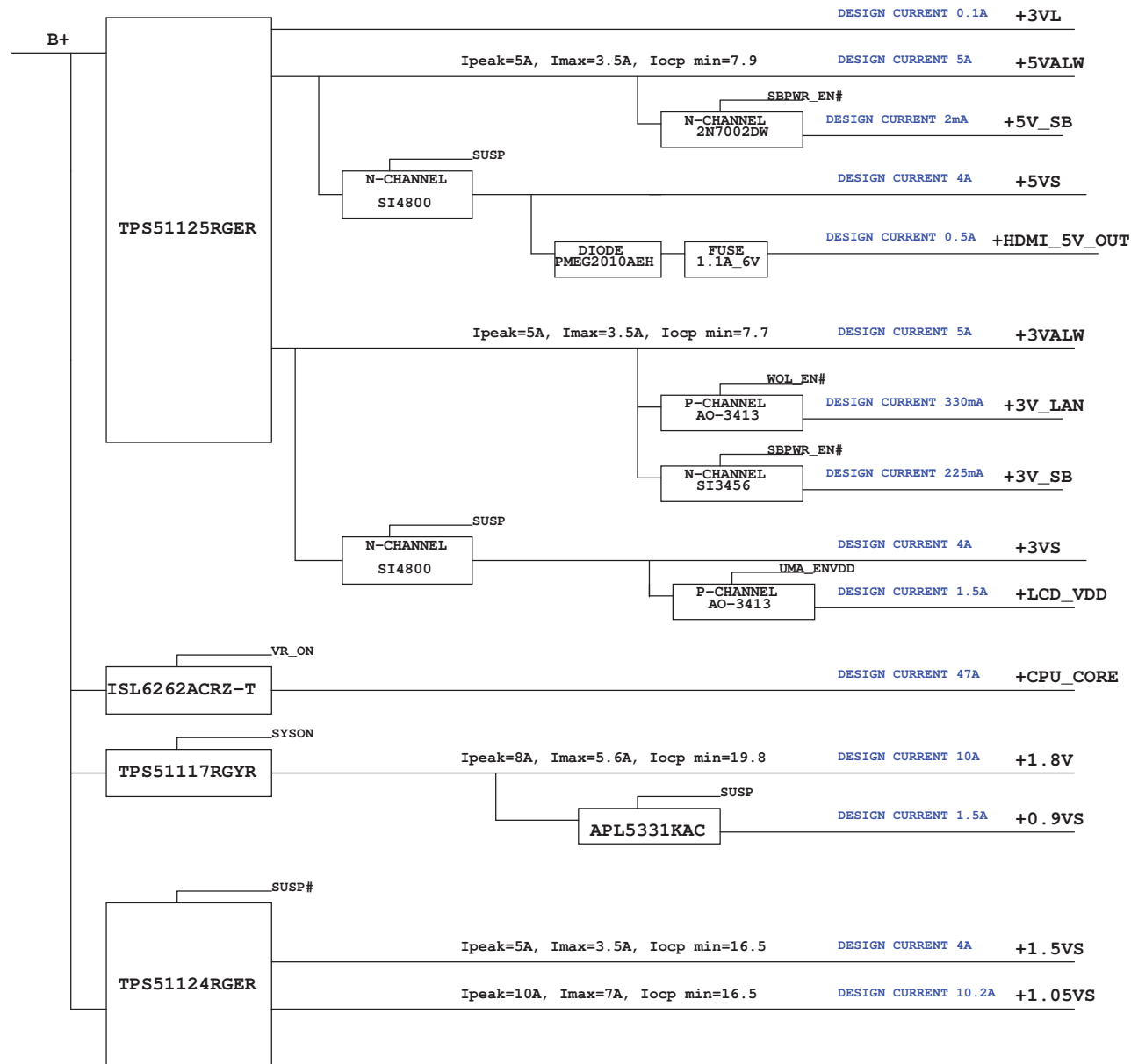
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Model Name : NBWAA

File Name : LA-5821P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	North Bridge		RJ11	CAMERA	MIC	HDMI	
description	GM	GL				Y	
explain	GM45	GL40	MODEM	CAMERA	MIC	HDMI	Non-HDMI
BTO	GM45R3@ GM45R1@	GL40R3@ GL40R1@	MDC@	CAM@	MIC@	IHDMI@	NIHDMI@

External PCI Devices

EC SM Bus1 address

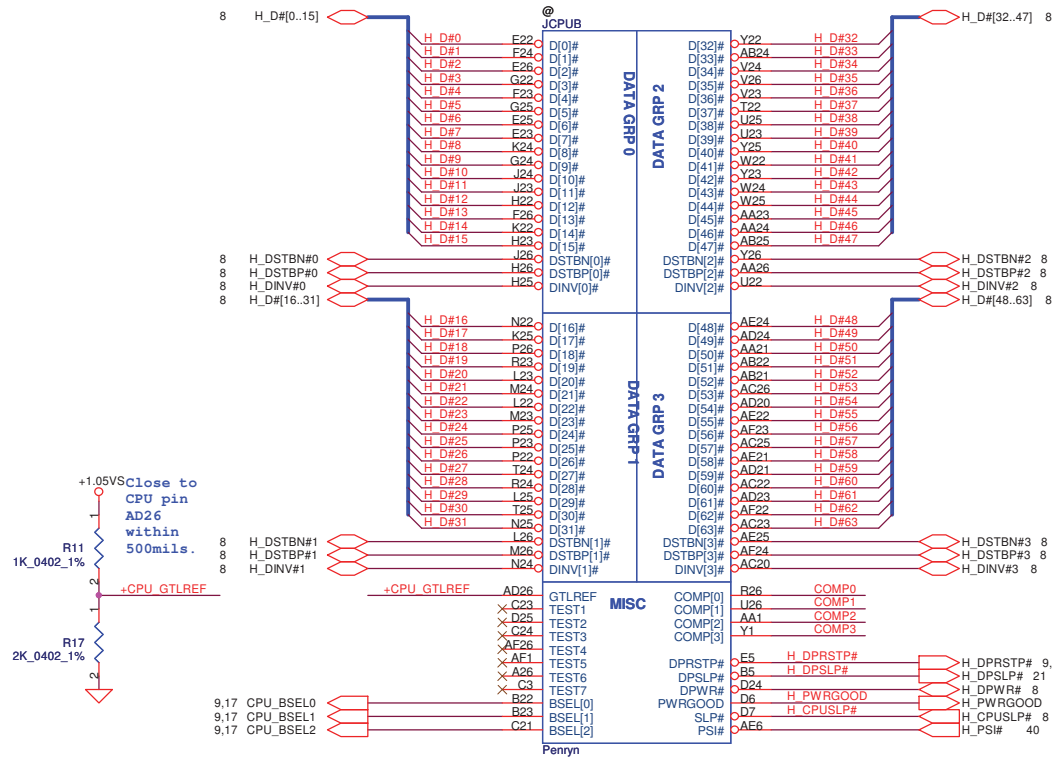
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011X b		CPU THM Sen	
+3VL	FUN/B (CAP Sensor)		+3VS	SMSC SMC1402	0100 110x b

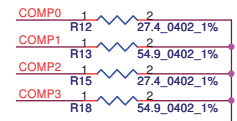
ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS		

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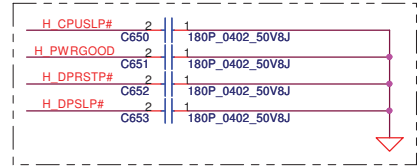
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



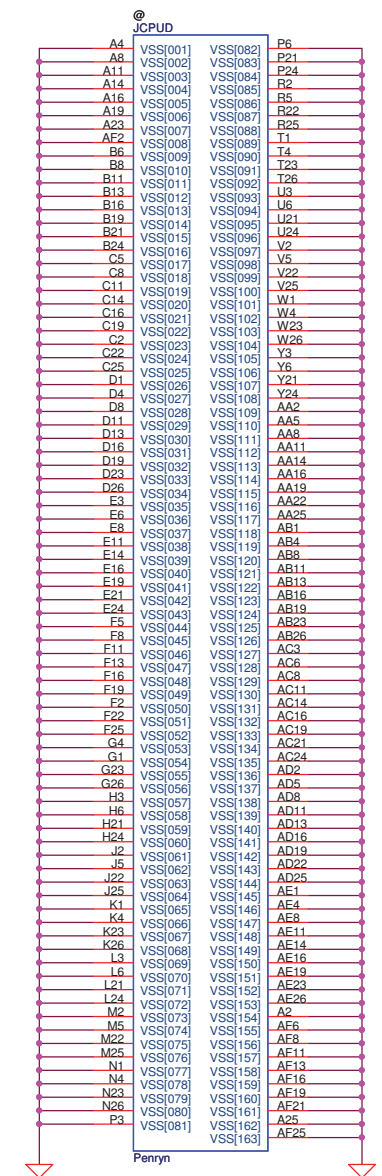
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

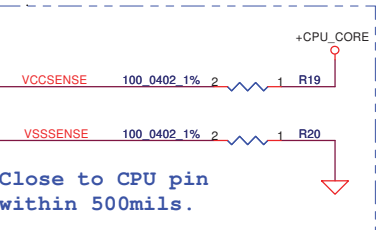
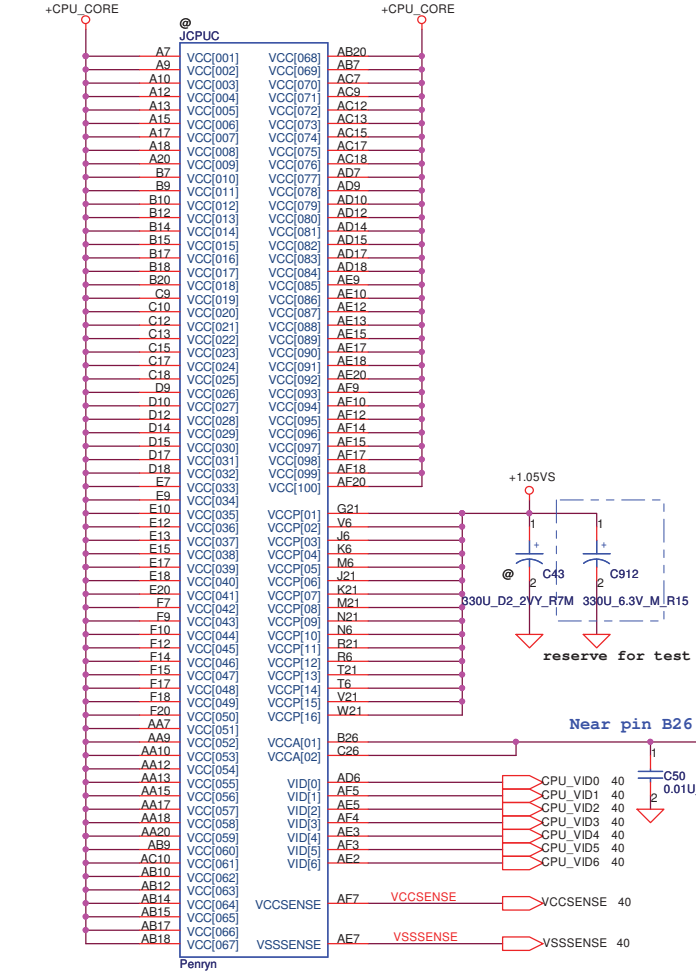
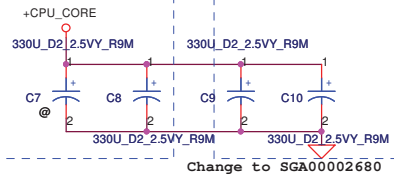


Reserve for debug close to CPU

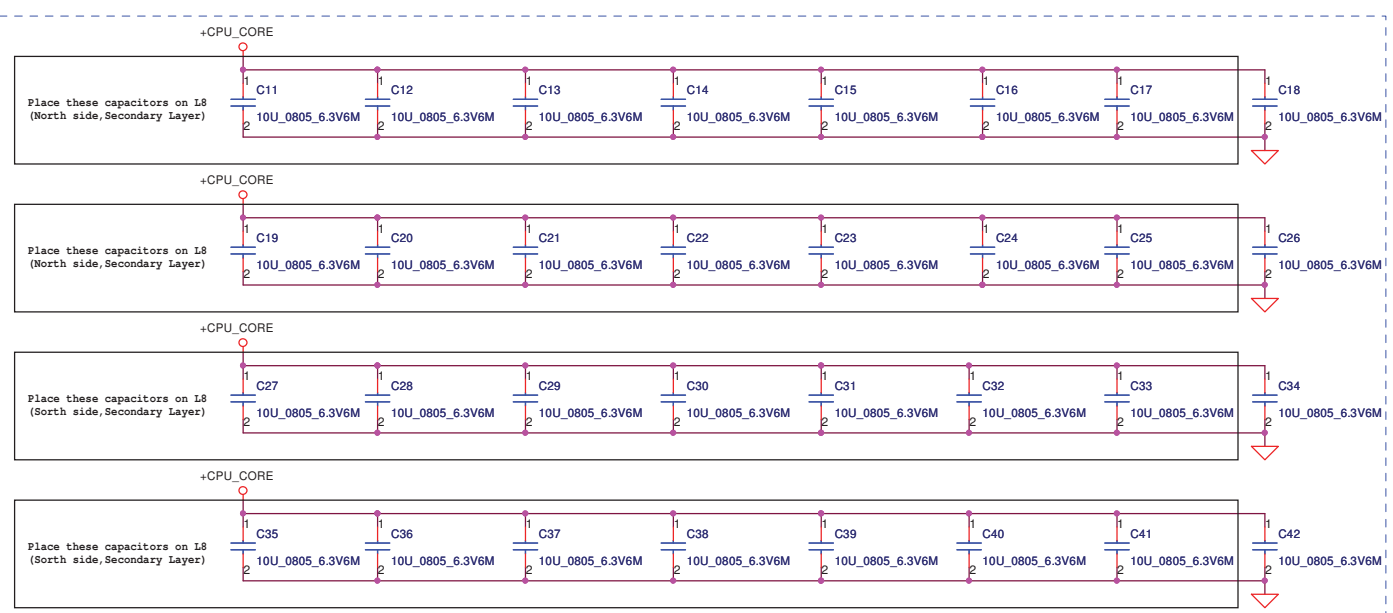


Near CPU CORE regulator

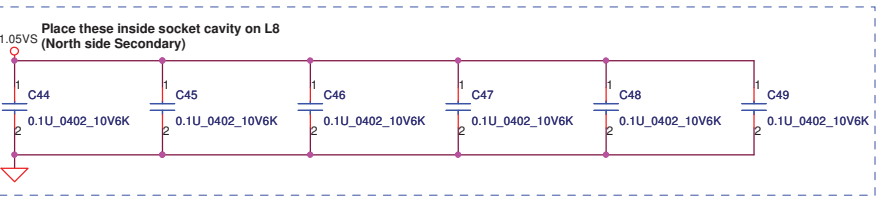
ESR <= 1.5m ohm
Capacitor > 1980uF



Length match within 25 mils.
The trace width/space/other is 14/7/25.

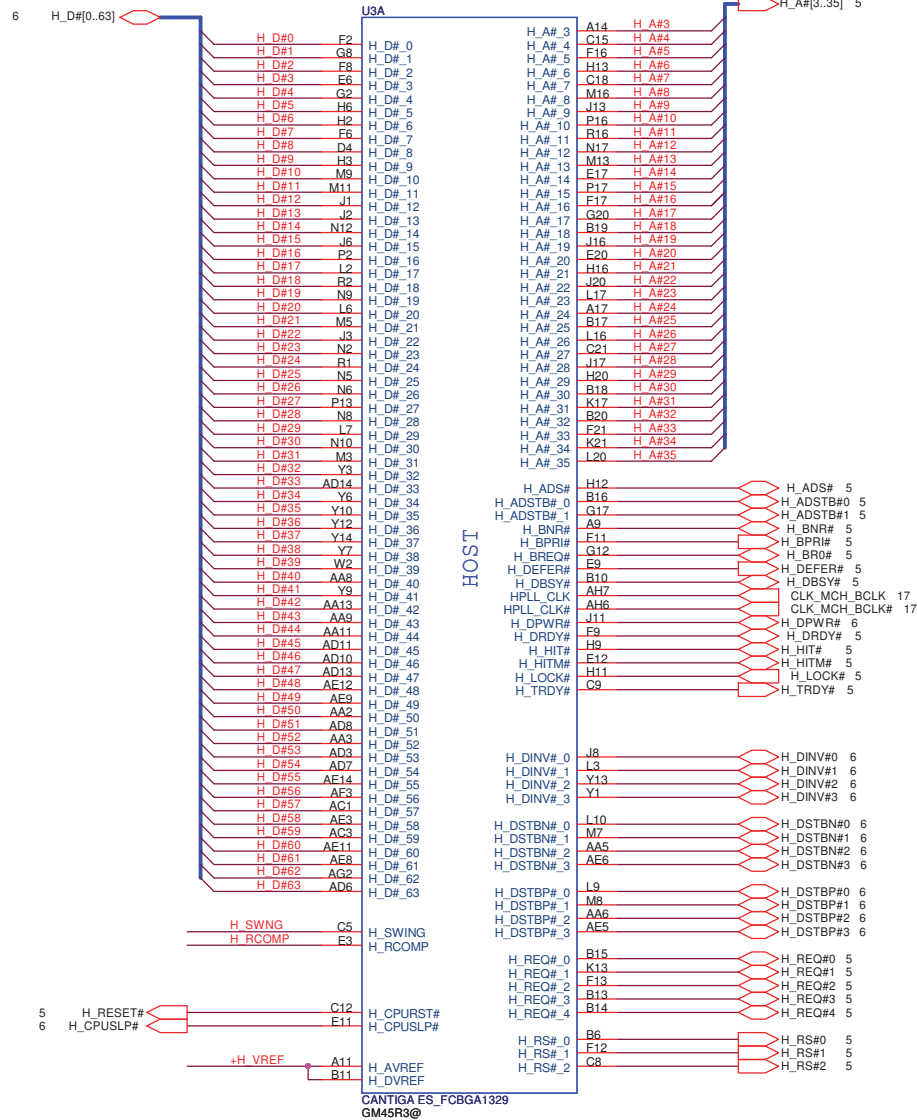
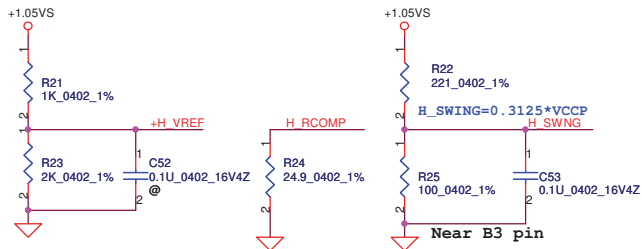


Mid Frequency Decoupling



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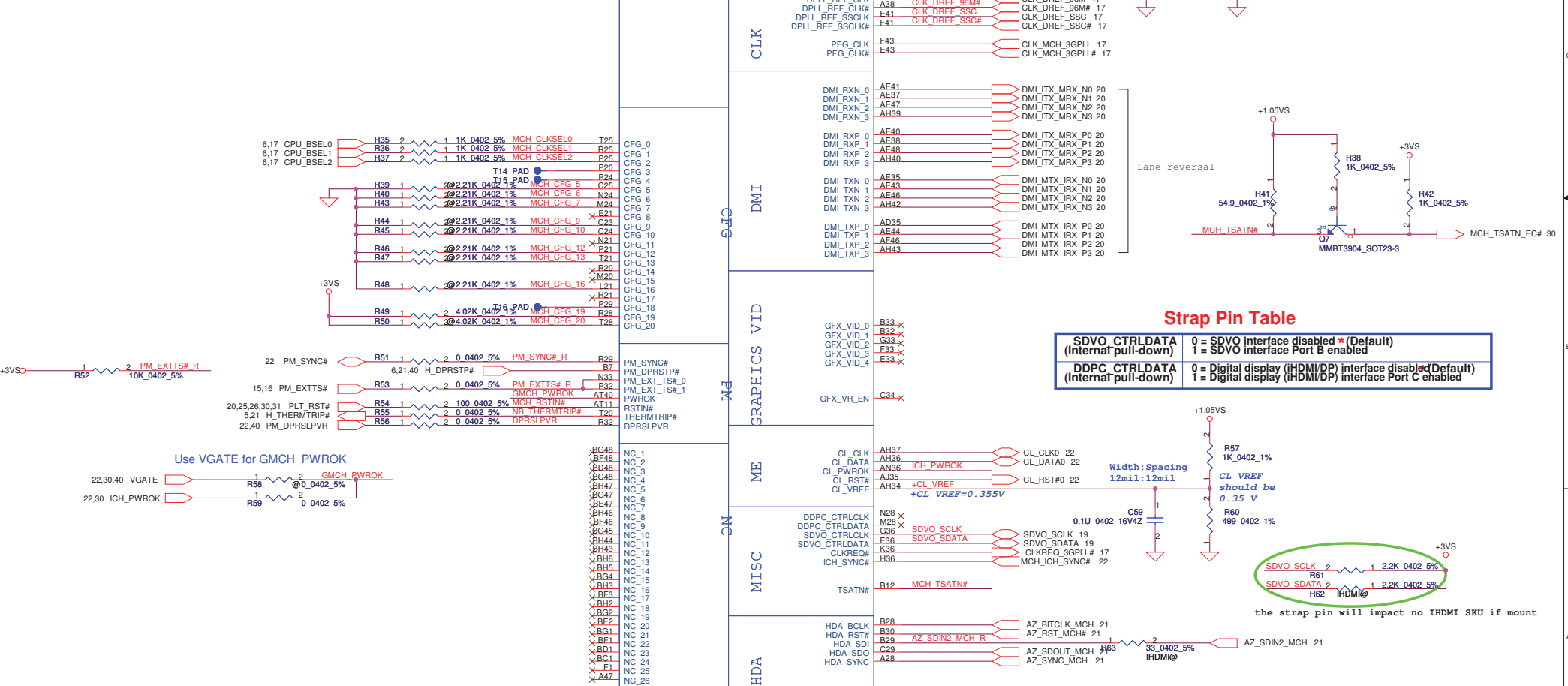
Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB



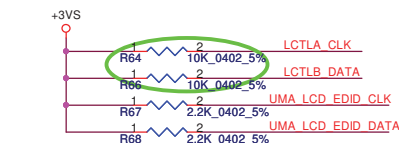
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Strap Pin Table

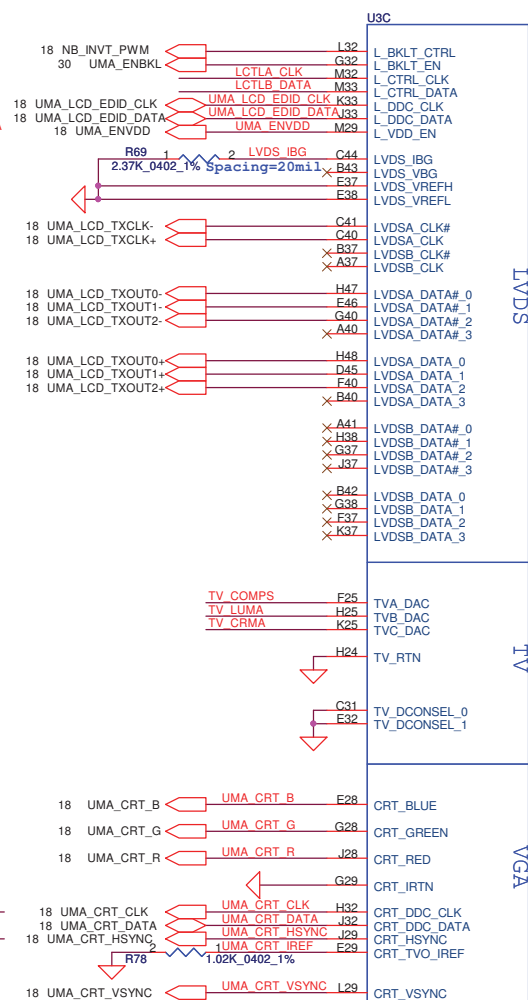
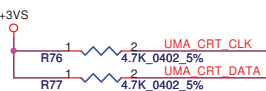
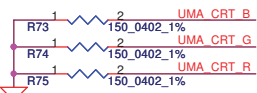
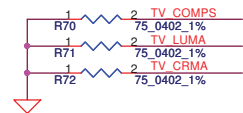
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = ITPM Host Interface is enabled can support disble by SW. 1 = ITPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface Port B enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (IHDMI/DP) interface disabled*(Default) 1 = Digital display (IHDMI/DP) interface Port C enabled



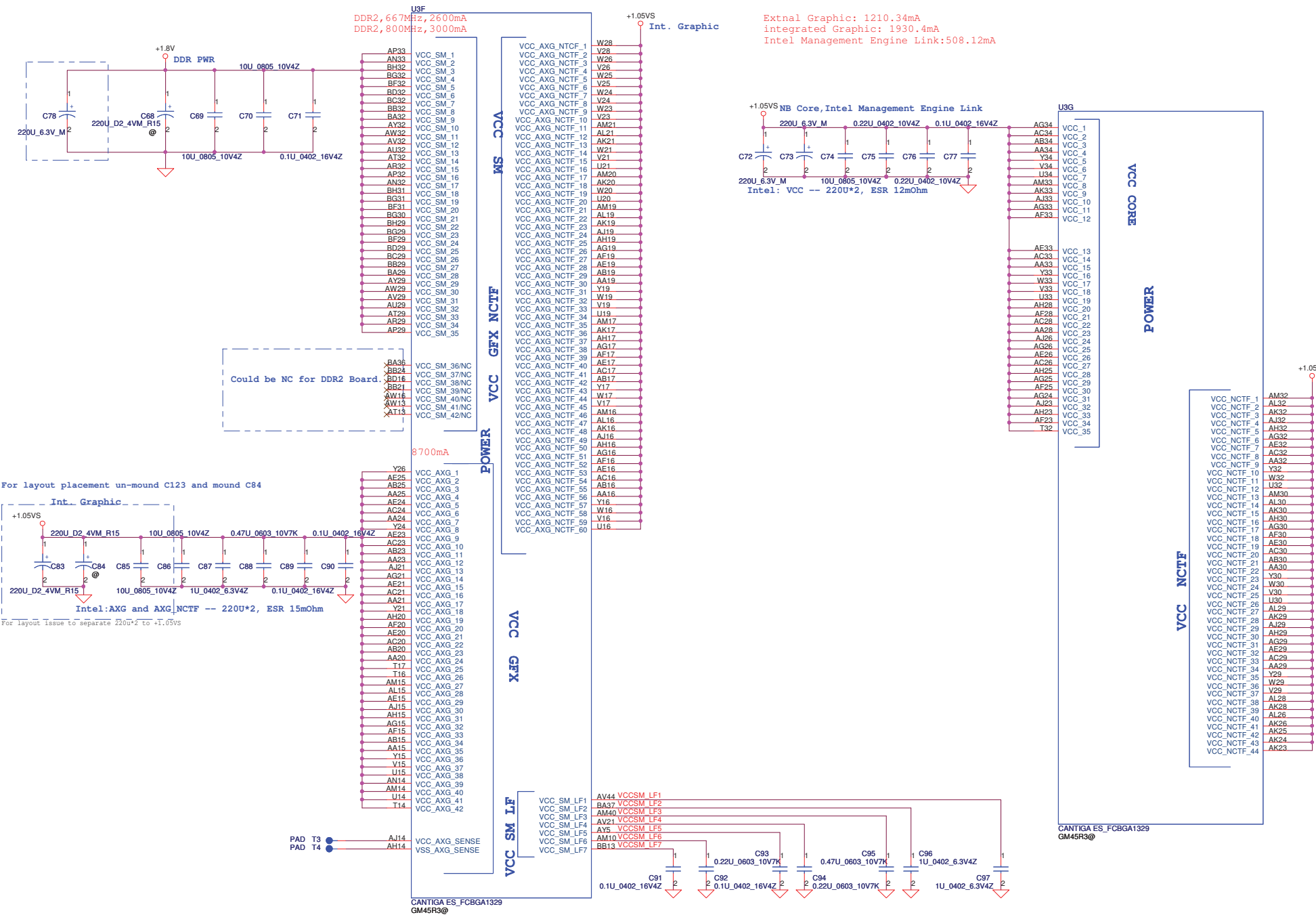
L_DDC_DATA
 0 = LFP Disable
 1 = LFP Card Present; PCIE disable



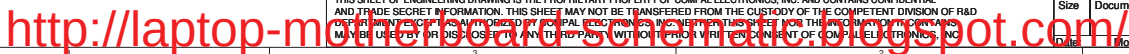
CANTIGA ES_FCBGA1329
 GM45R3@

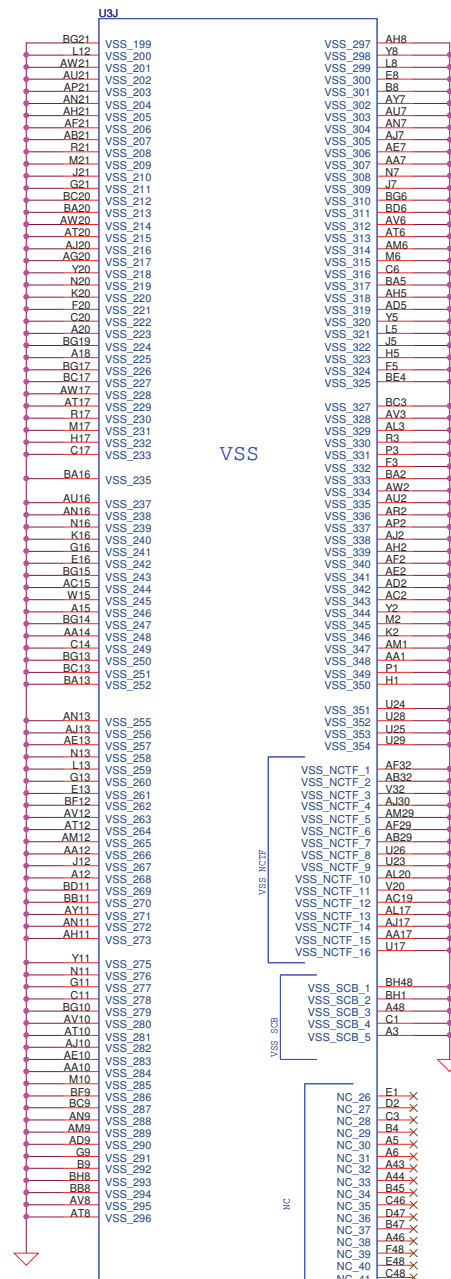
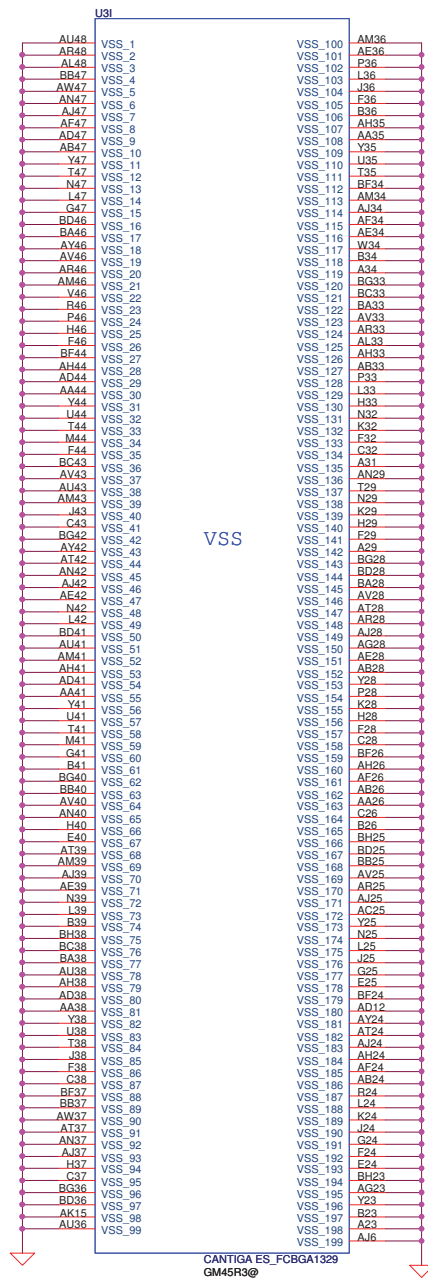
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<http://laptop-motherboard-schematic.blogspot.com/>

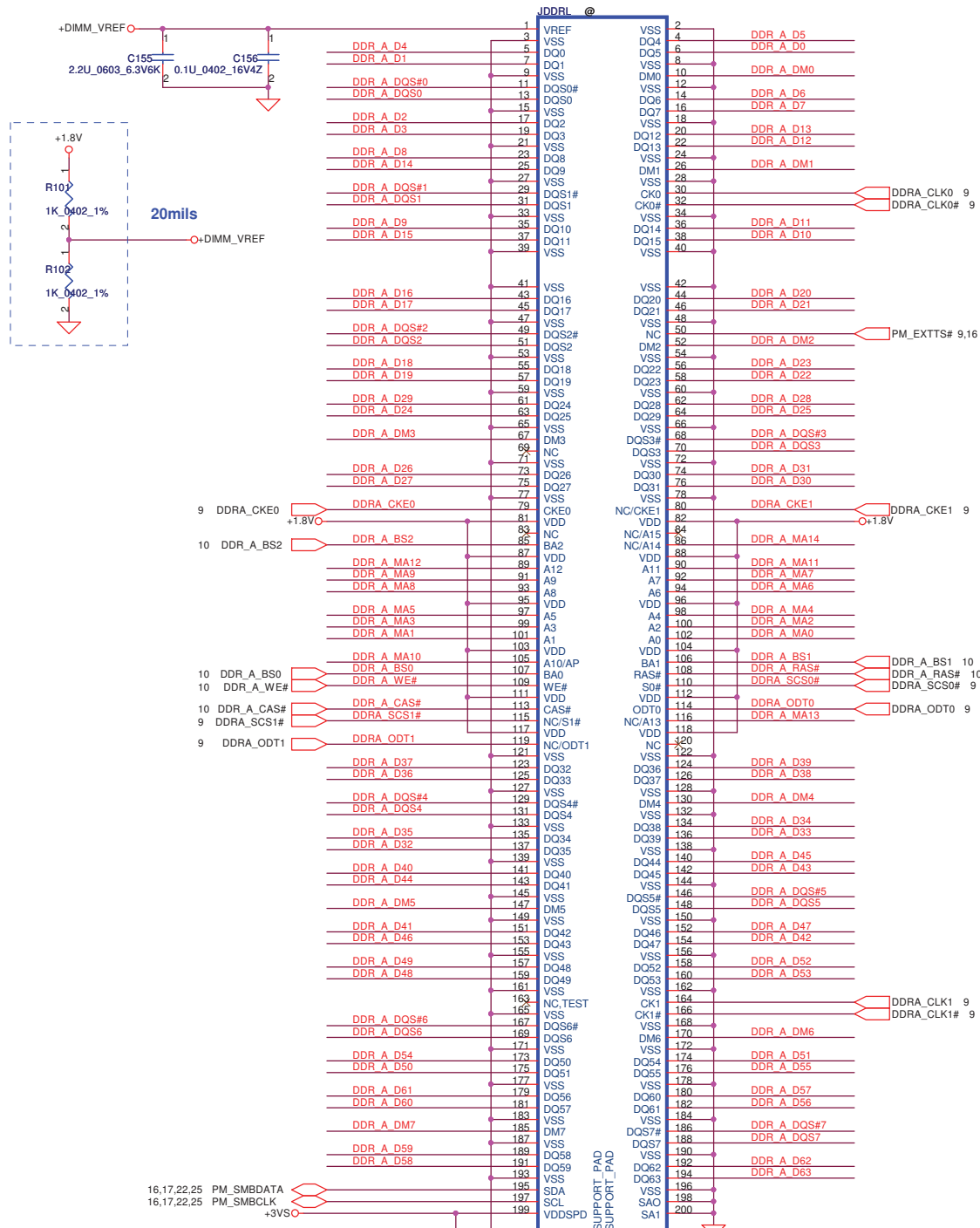


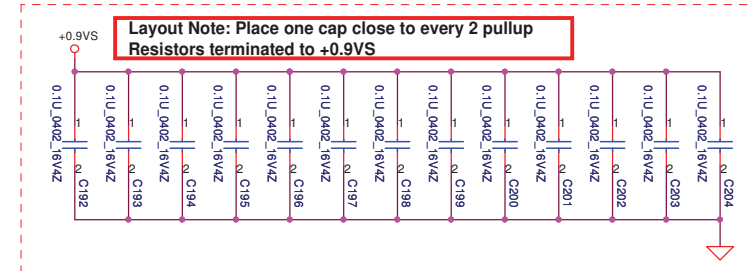
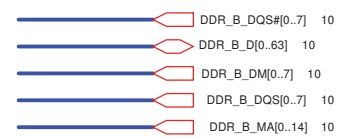
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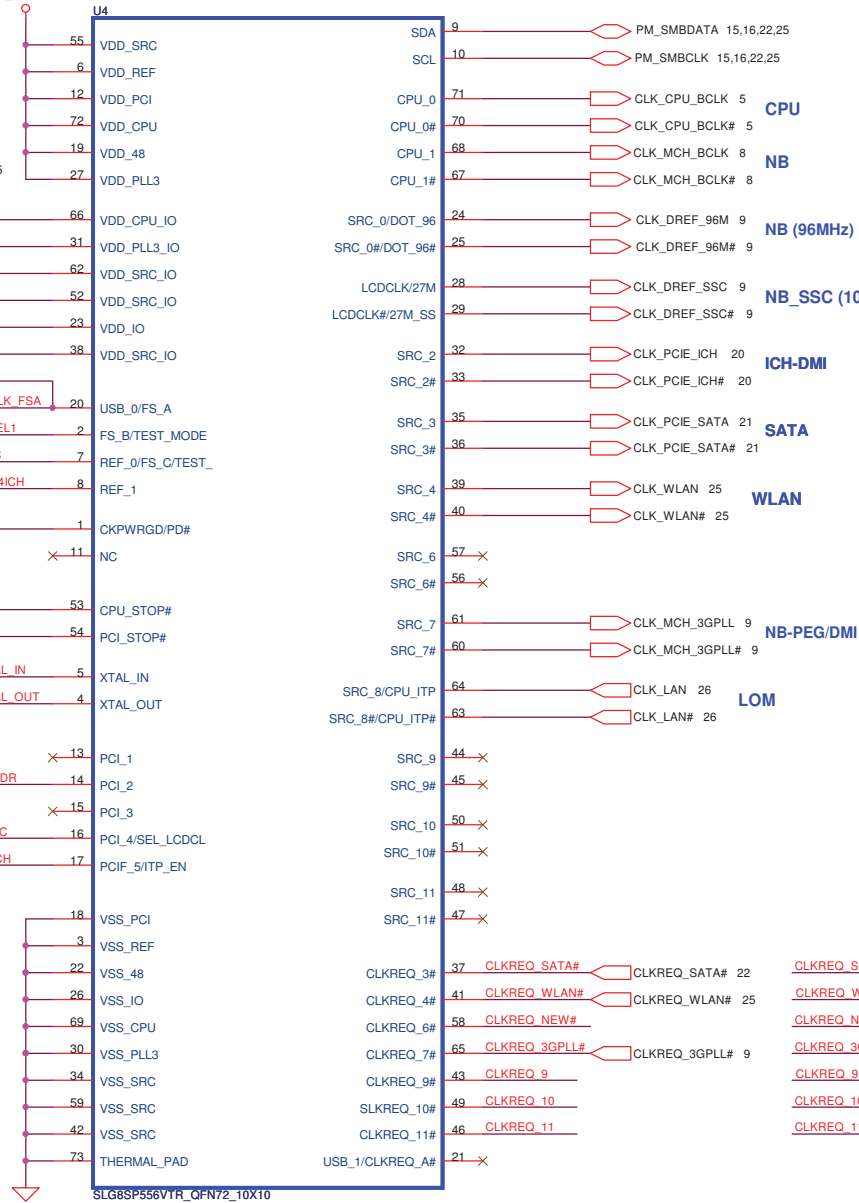
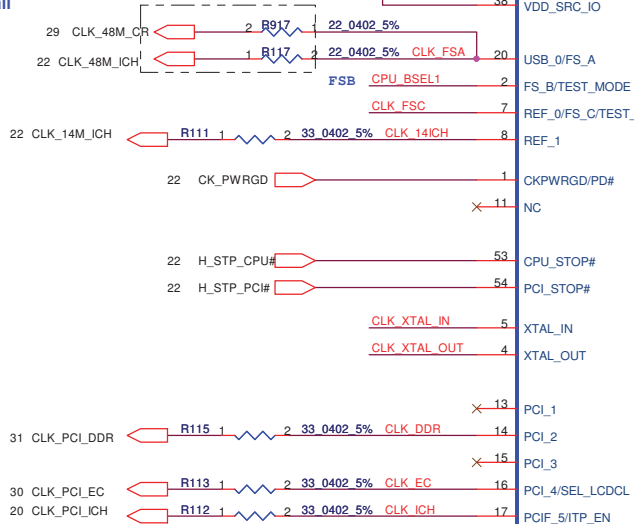
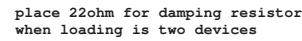
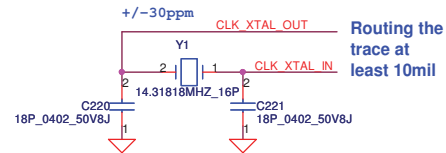
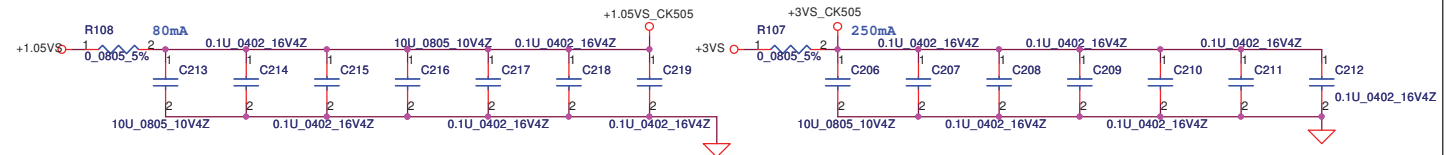


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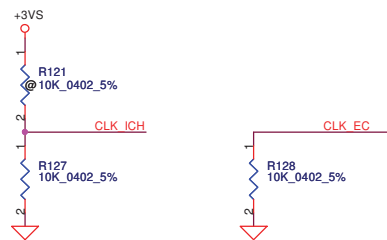
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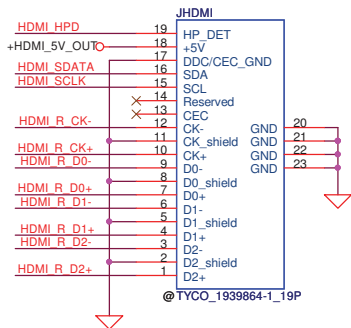
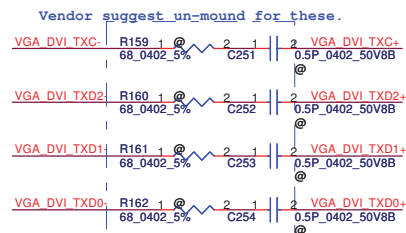
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



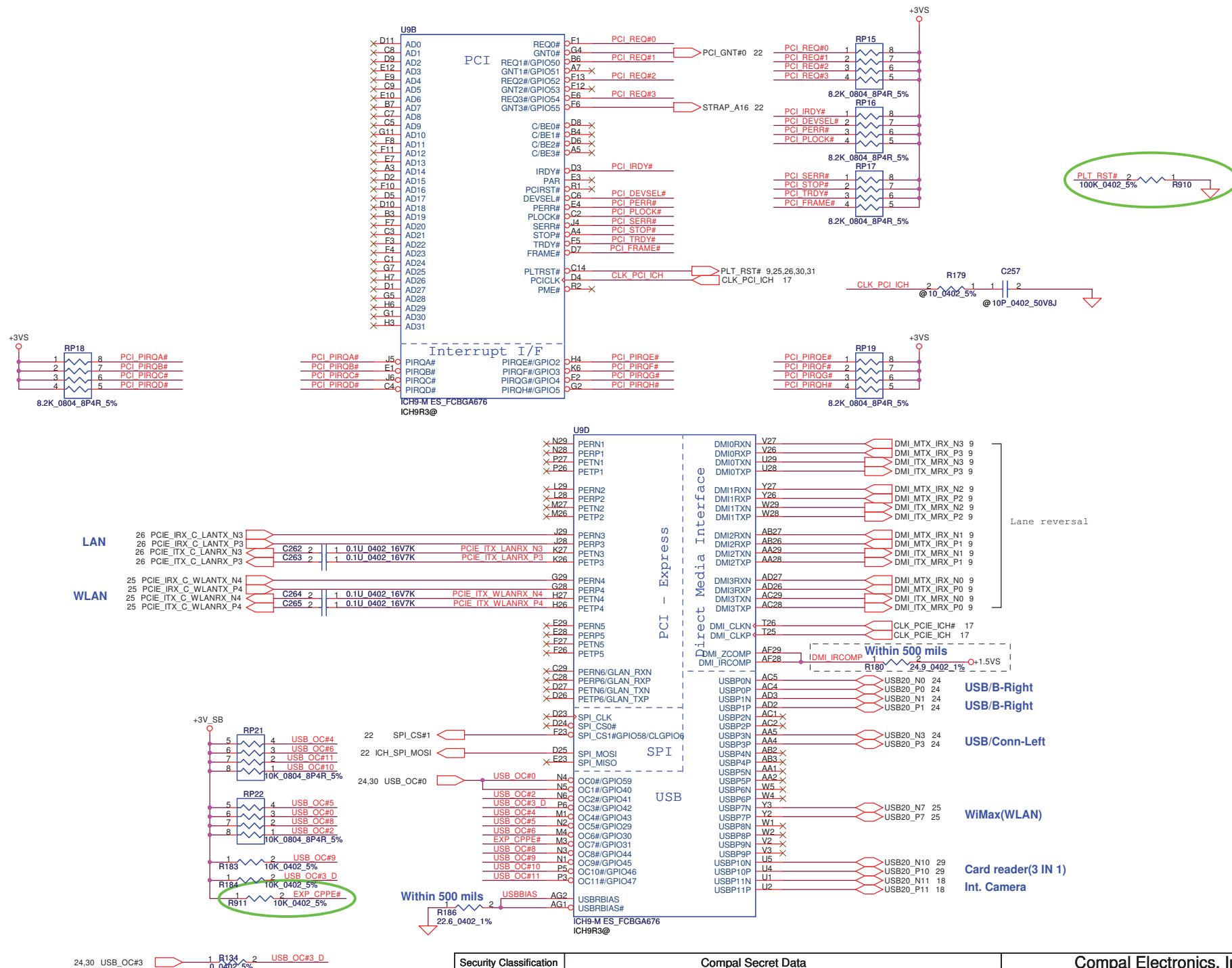
CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



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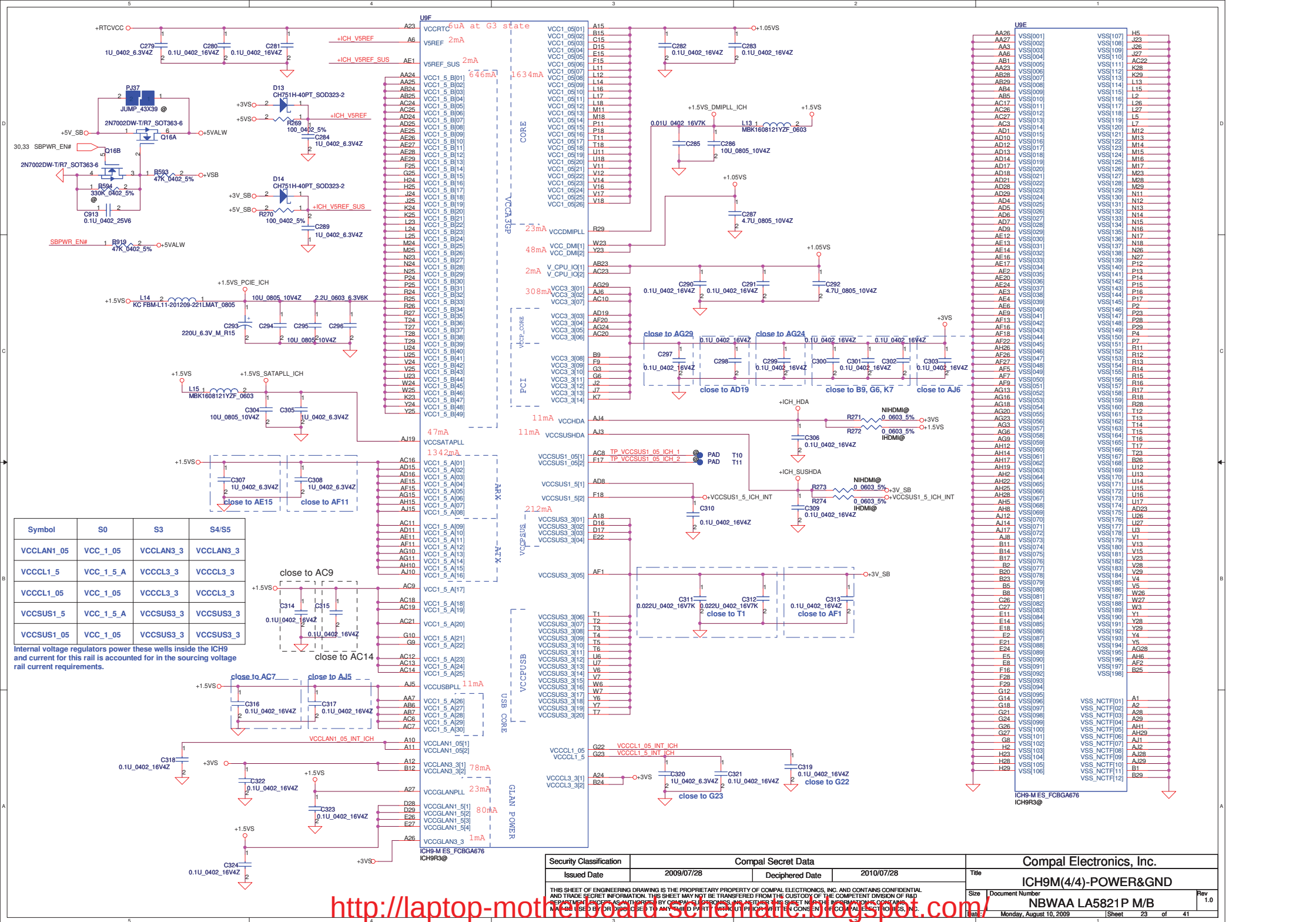


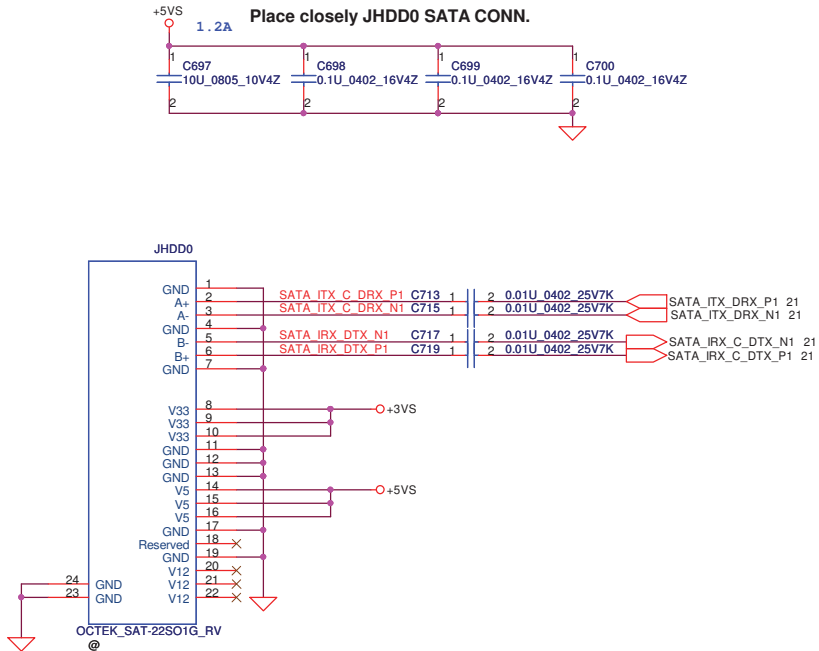
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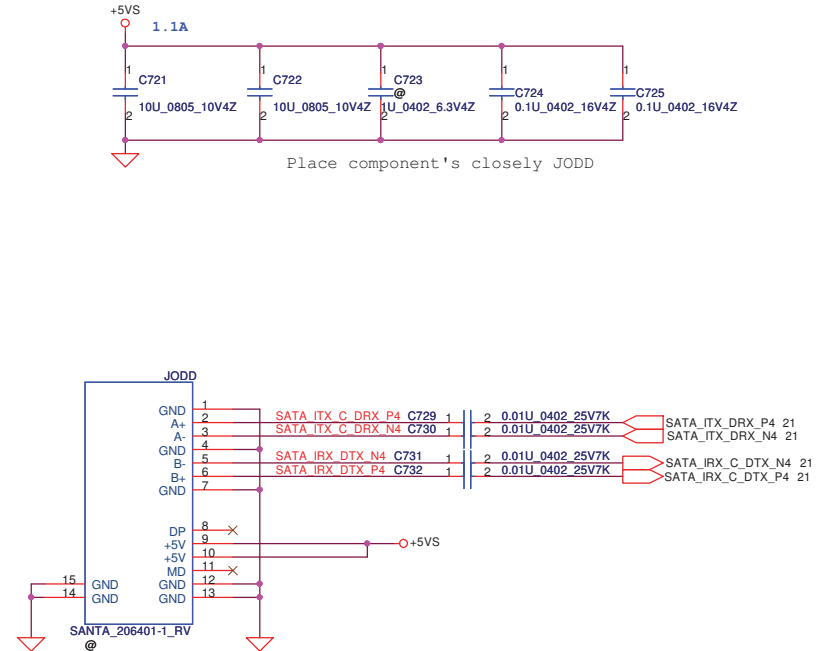
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Issued Date		2009/07/28		Deciphered Date		2010/07/28	
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				ICH9M(1/4)-PCI			
				Size		Document Number	
				NBWAA LA5821P M/B		1.0	
				Date:		Monday, August 10, 2009	
				Sheet		20 of 41	

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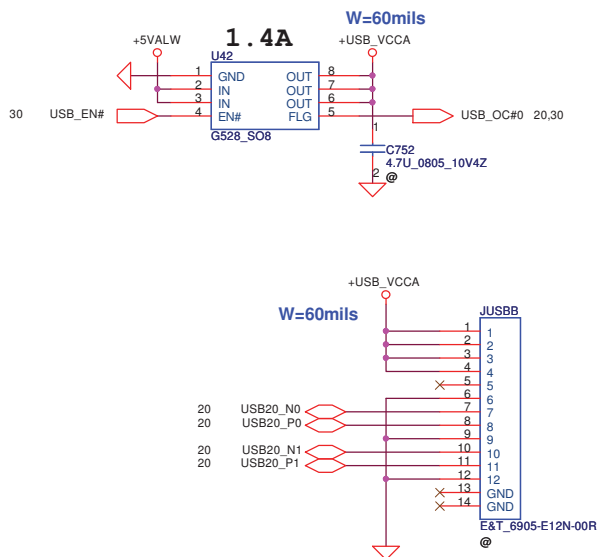


SATA HDD Conn.

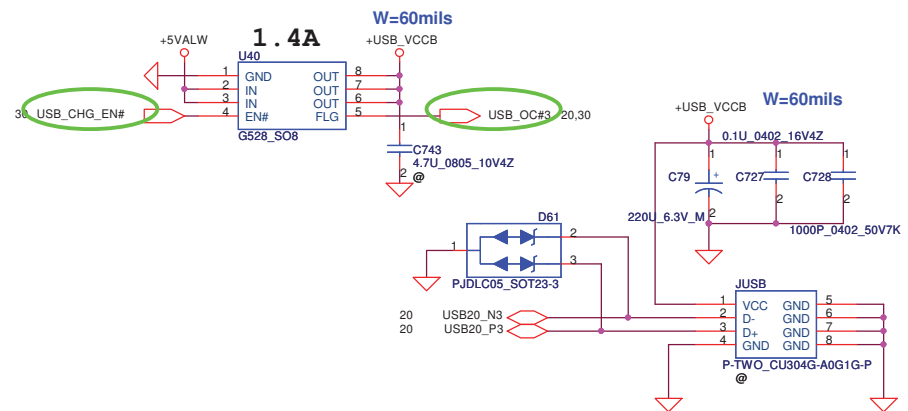
SATA ODD Conn



USB Board Conn

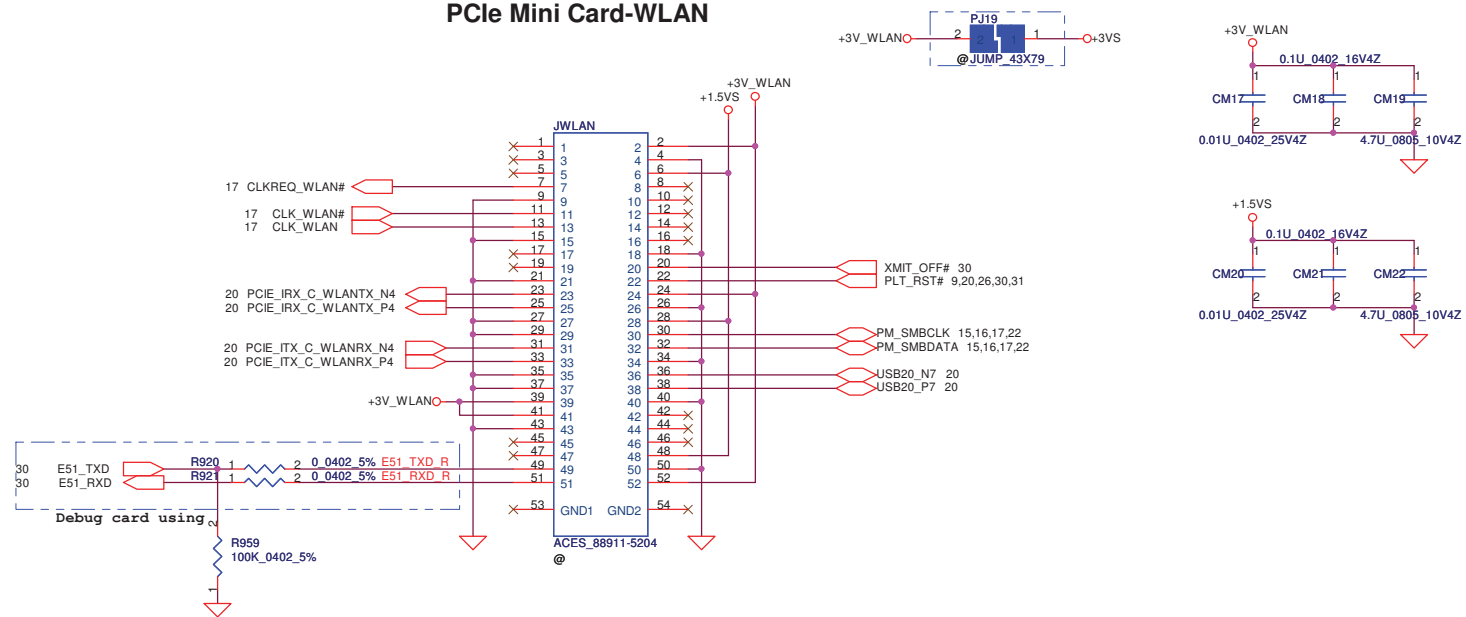


USB Left Conn

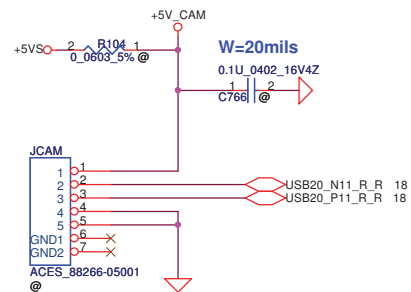


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Issued Date	2009/07/28	Deciphered Date	2010/07/28	Title			
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				Size	Document Number	Rev	
				NBWAA LA5821P M/B			1.0
Date:		Thursday, August 06, 2009		Sheet		24	of 41

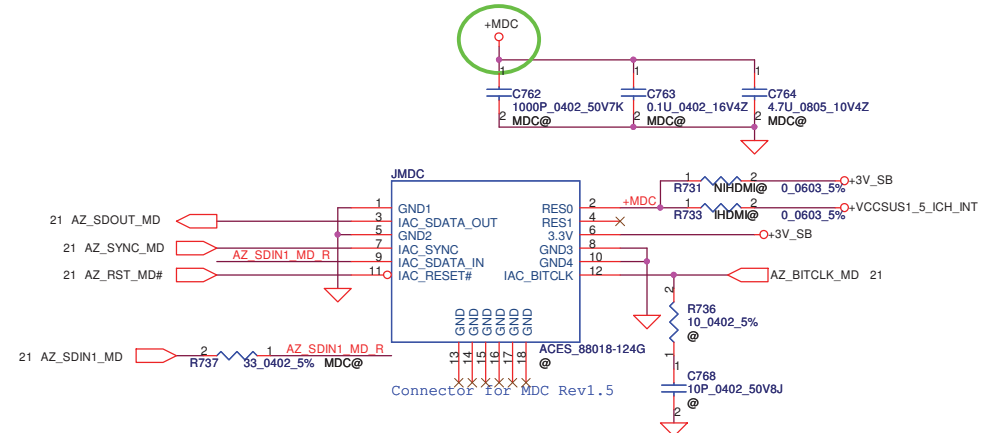
PCIe Mini Card-WLAN



Int. Camera

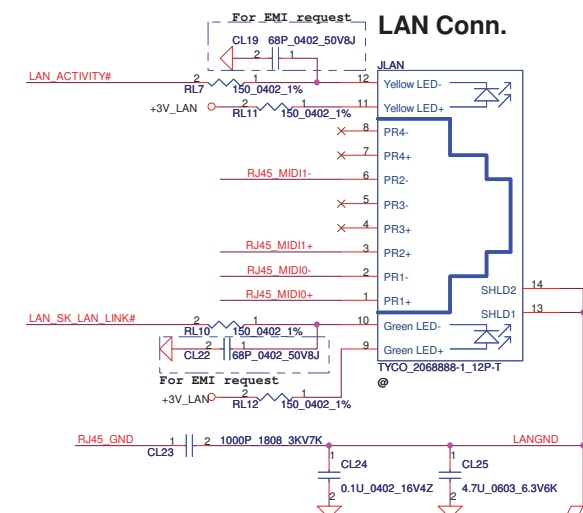
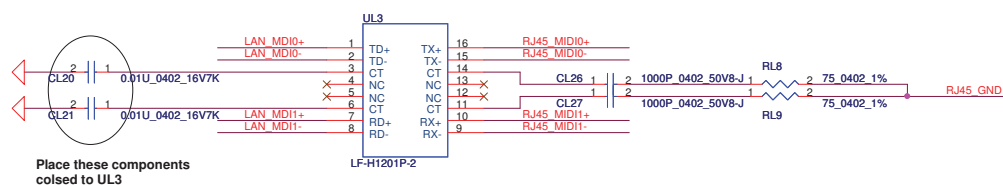
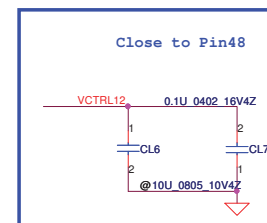
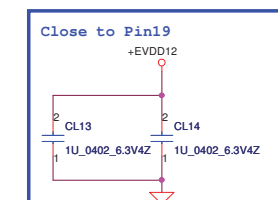
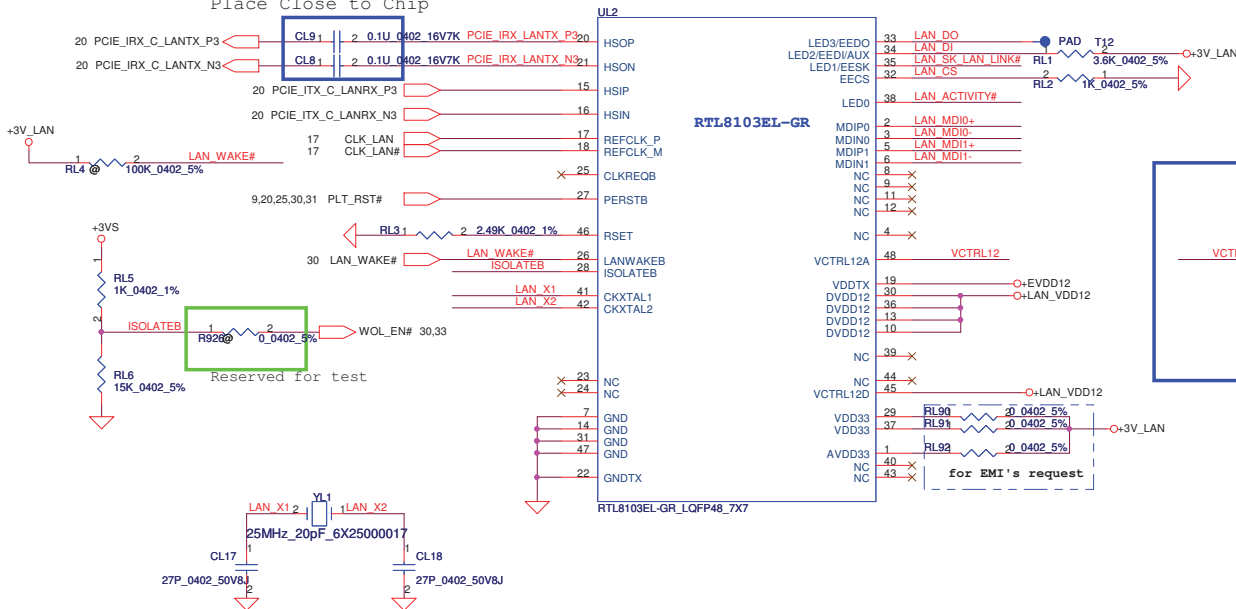


MDC 1.5 Conn.



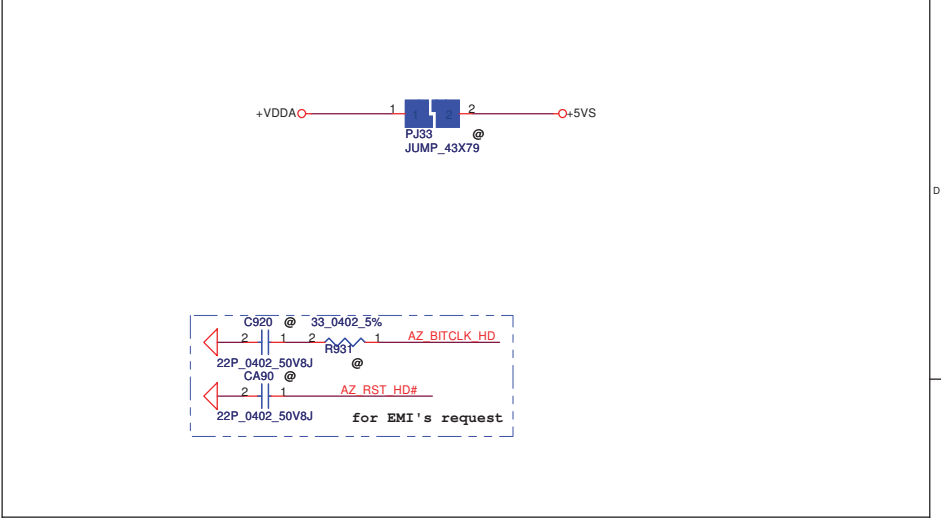
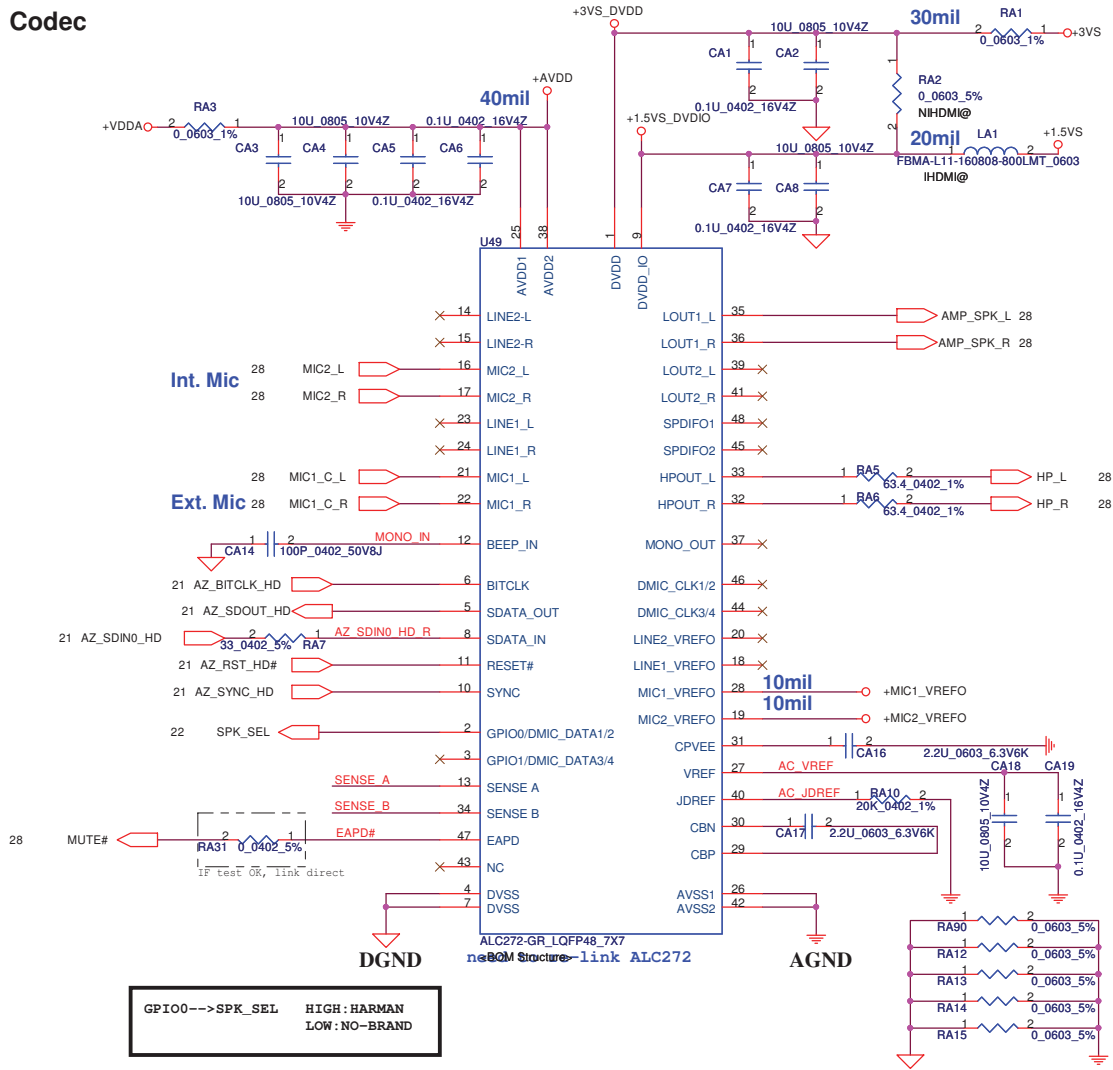
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Issued Date				2009/07/28		Deciphered Date		2010/07/28		Title	
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										NBWAA LA5821P M/B	
										Rev 1.0	
										Date: Monday, August 10, 2009	
										Sheet 25 of 41	

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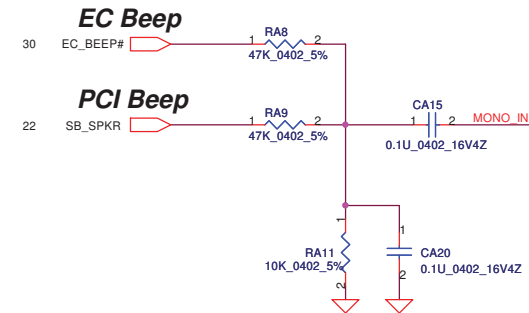


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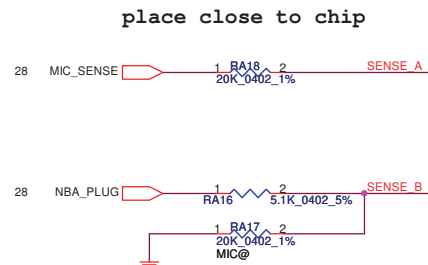
Codec



Beep sound

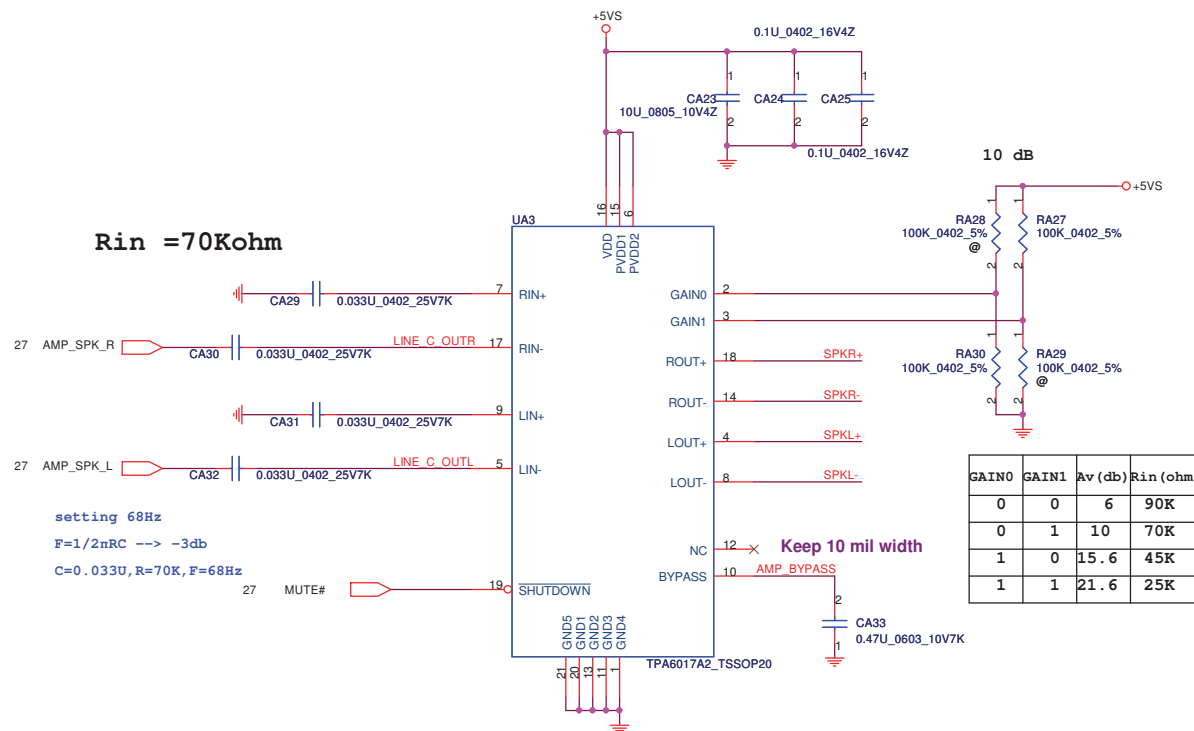


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

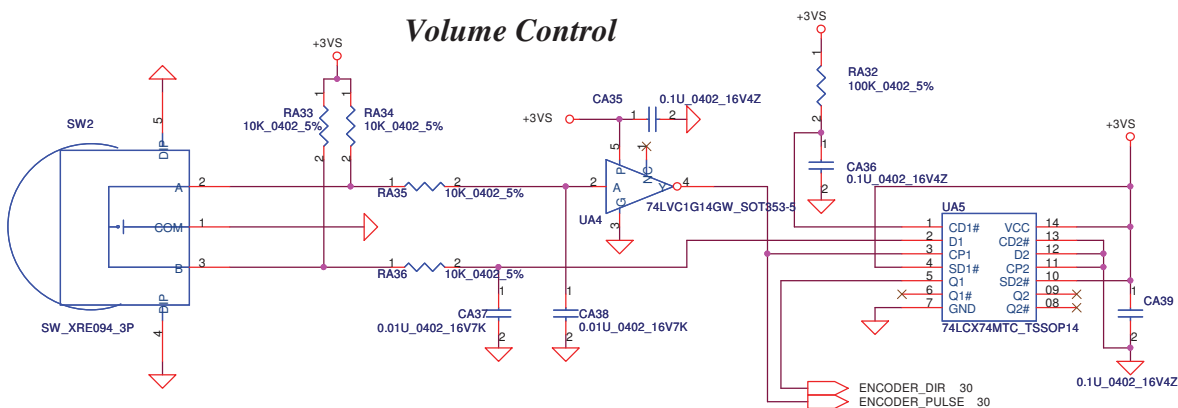


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2009/07/28				2010/07/28				Title			
2010/07/28				HD CODEC ALC272				Size			
Document Number				NBWAA LA5821P M/B				Rev			
1.0				Date				Monday, August 10, 2009			
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41											

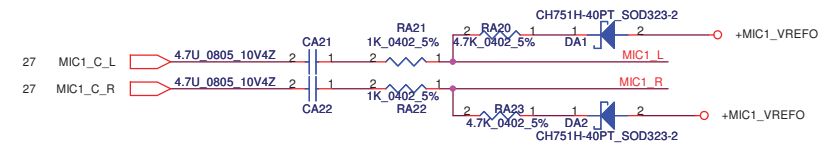
TPA6017 Medium Range Amplifier



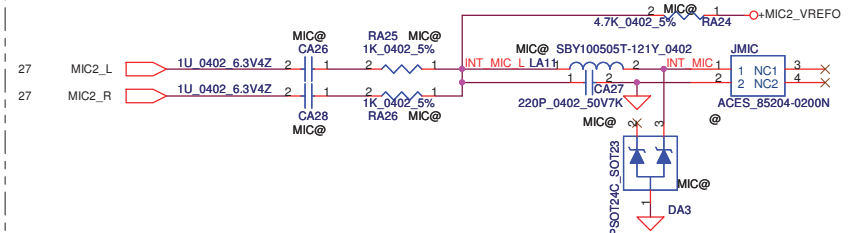
Volume Control



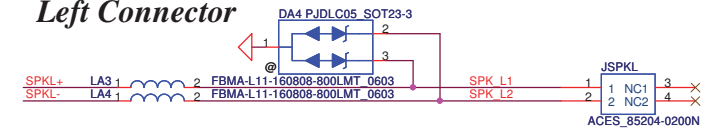
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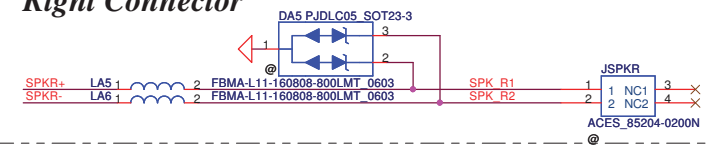
Int. Mic



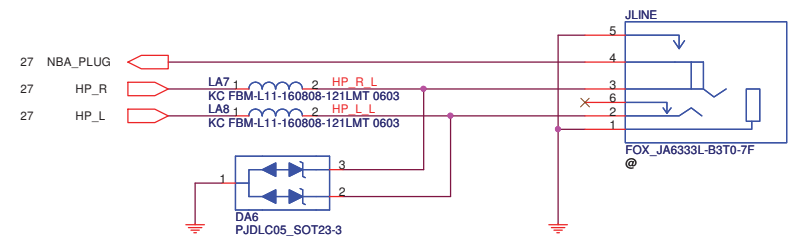
Left Connector



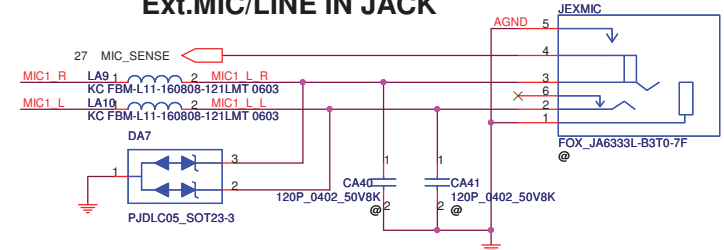
Right Connector



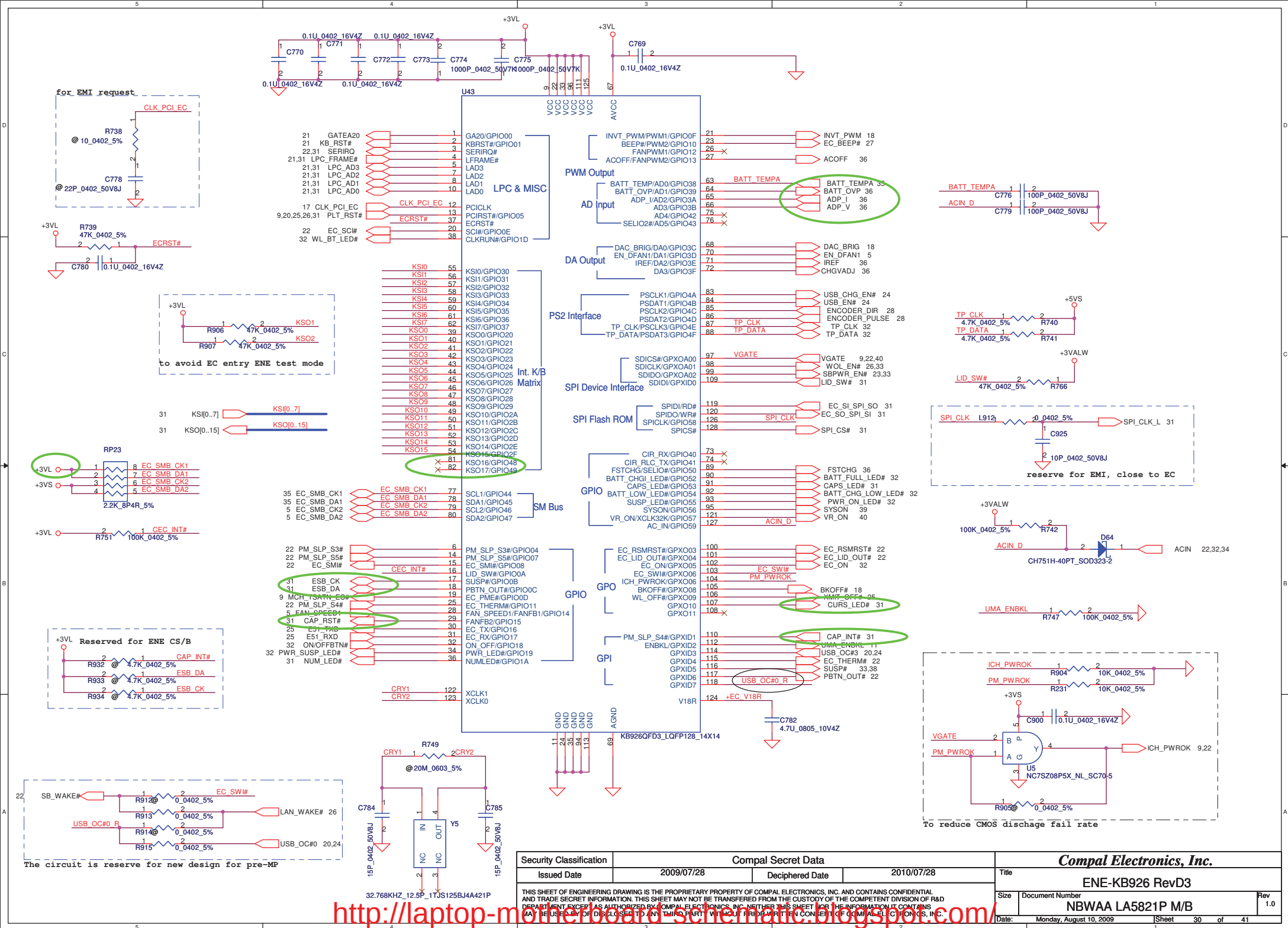
HeadPhone/LINE Out JACK



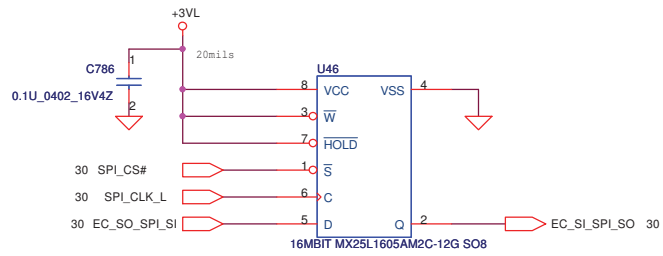
Ext.MIC/LINE IN JACK



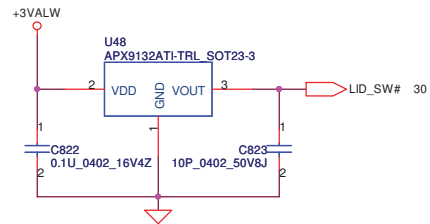
Security Classification		Compal Secret Data		Title	
Issued Date	2009/07/28	Deciphered Date	2010/07/28	AUDIO AMP/MIC/SPK/VR	
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SPI Flash (16Mb*1)

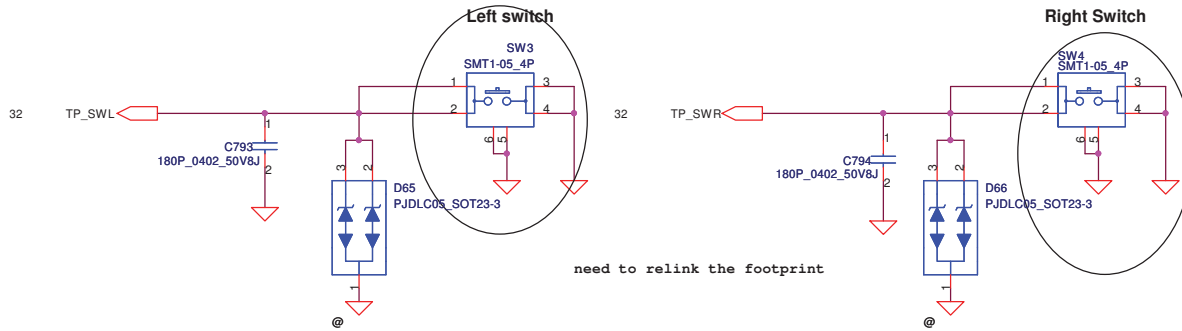
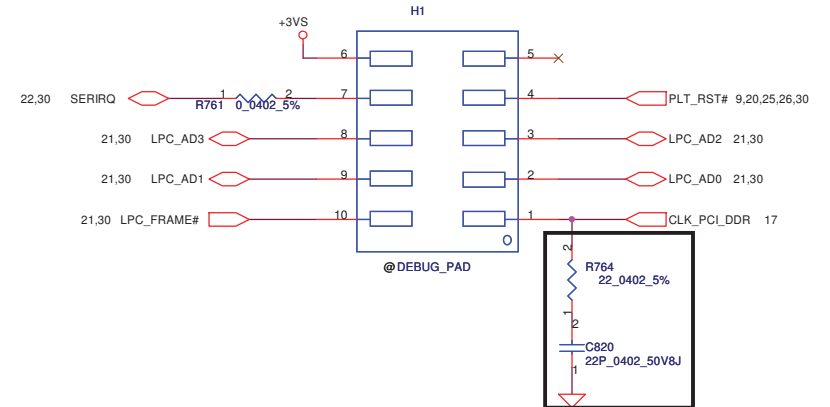


Lid SW

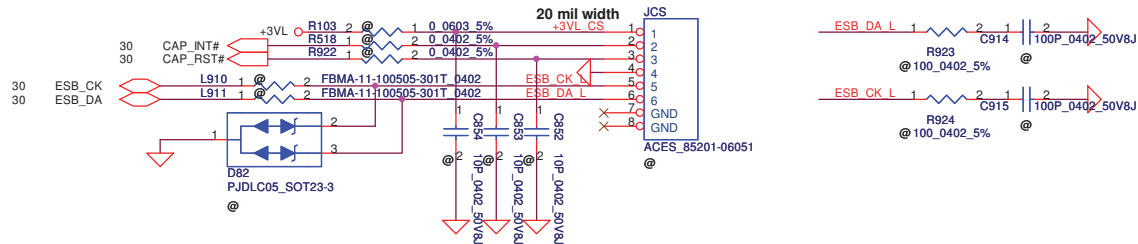


LPC Debug Port

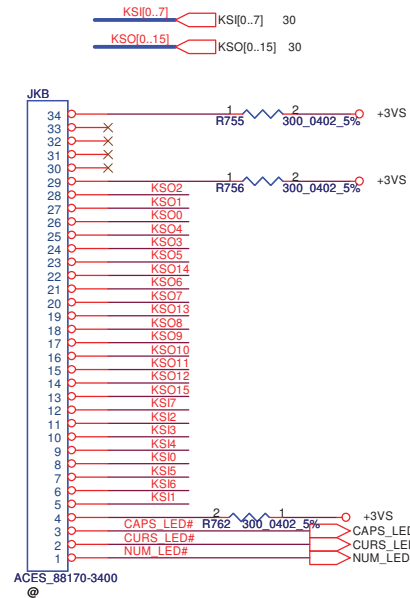
Please place the PAD under DDR DIMM.



CS/B Connector



KEYBOARD
CONN .

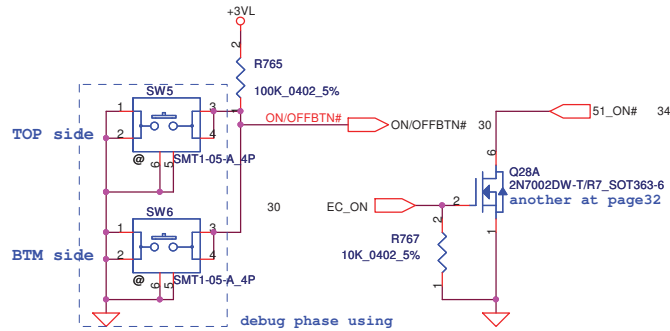


| please close to JKB

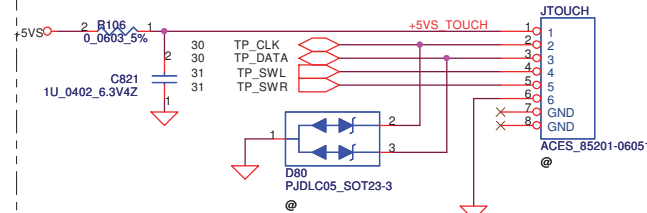
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<u>KSO0</u>	C790	100P_0402_50V8J
	1	2
<u>KSO4</u>	C791	100P_0402_50V8J
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<u>KSO3</u>	C792	100P_0402_50V8J
	1	2
<u>KSO5</u>	C795	100P_0402_50V8J
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<u>KSO14</u>	C796	100P_0402_50V8J
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<u>KSO6</u>	C797	100P_0402_50V8J
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<u>KSO7</u>	C798	100P_0402_50V8J
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<u>KSO13</u>	C799	100P_0402_50V8J
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<u>KSO8</u>	C800	100P_0402_50V8J
	1	2
<u>KSO9</u>	C801	100P_0402_50V8J
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<u>KSO12</u>	C804	100P_0402_50V8J
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<u>KSO15</u>	C805	100P_0402_50V8J
	1	2
<u>KS17</u>	C807	100P_0402_50V8J
	1	2
<u>KS12</u>	C808	100P_0402_50V8J
	1	2
<u>KS13</u>	C810	100P_0402_50V8J
	1	2
<u>KS14</u>	C811	100P_0402_50V8J
	1	2
<u>KS10</u>	C812	100P_0402_50V8J
	1	2
<u>KS15</u>	C813	100P_0402_50V8J
	1	2
<u>KS16</u>	C814	100P_0402_50V8J
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<u>KS11</u>	C815	100P_0402_50V8J
	1	2
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<u>CURS_LED#</u>	C817	100P_0402_50V8J
	1	2
<u>NUM_LED#</u>	C818	100P_0402_50V8J
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	C819	100P_0402_50V8J

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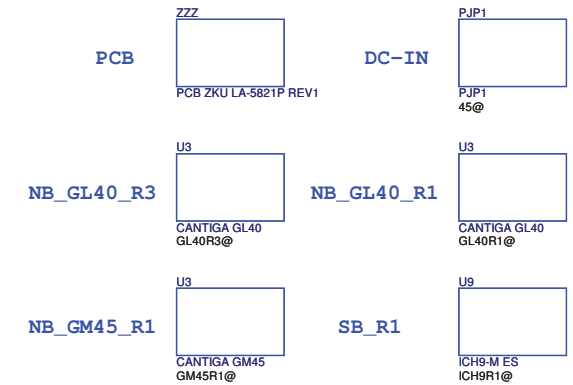
Power Button



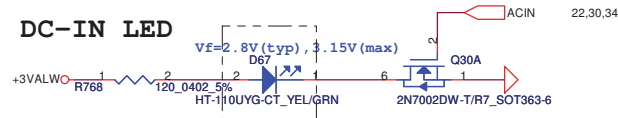
Touch Pad Connector



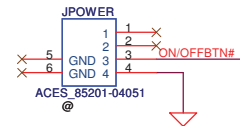
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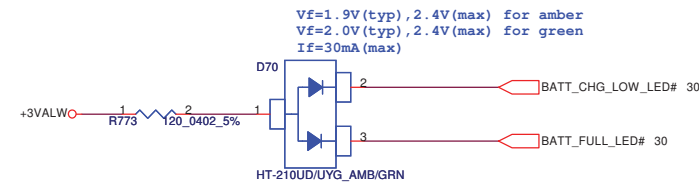
DC-IN LED



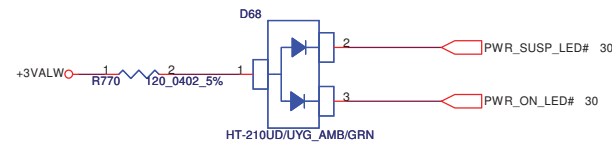
PWR/B



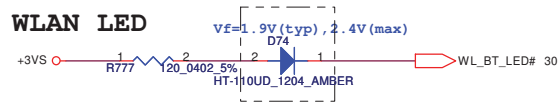
BATT CHARGE/FULL LED



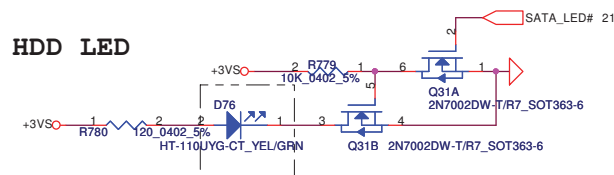
POWER/SUSPEND LED



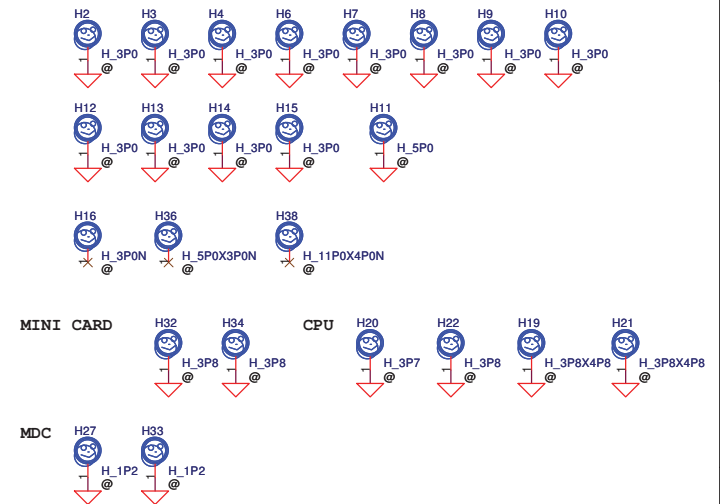
WLAN LED



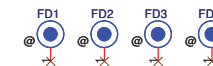
HDD LED



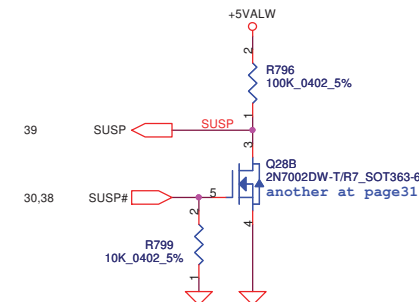
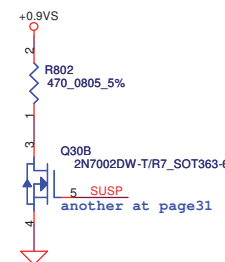
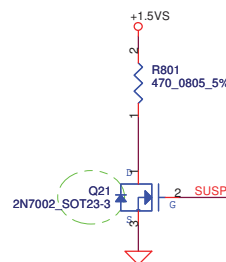
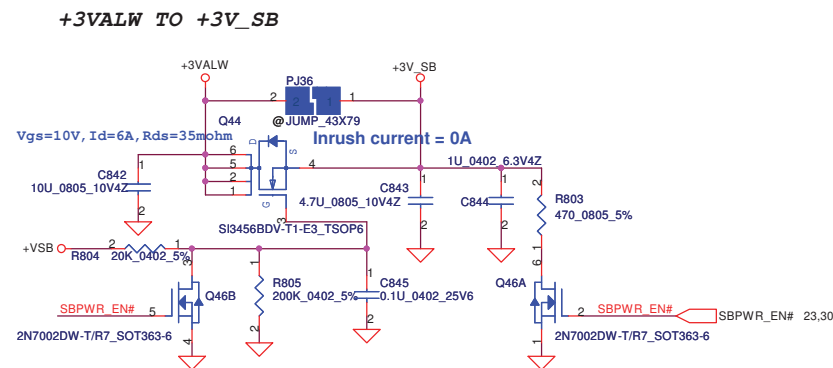
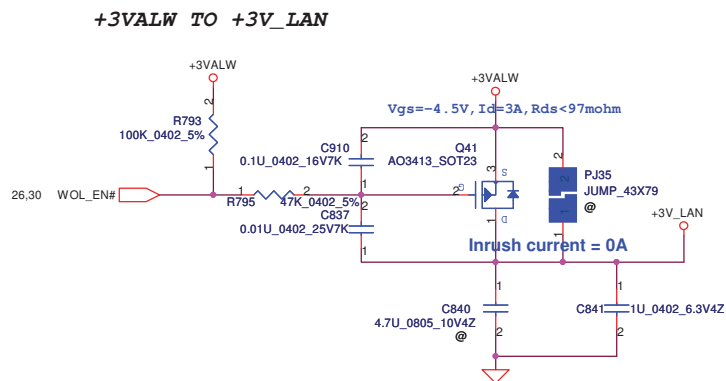
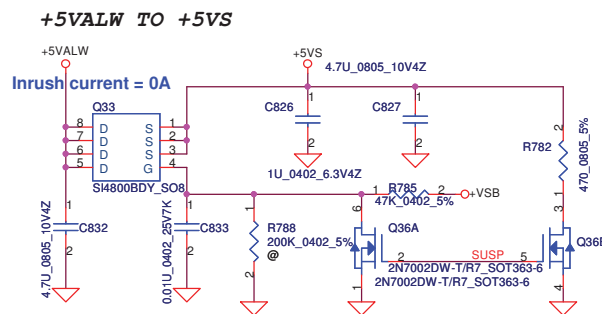
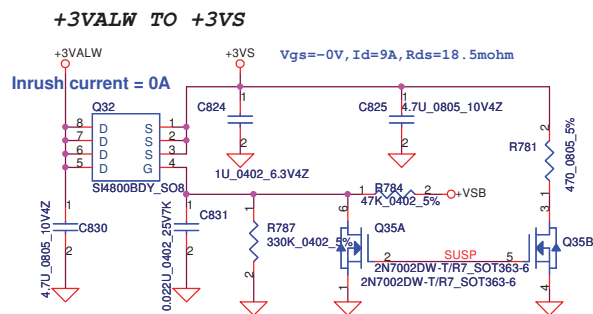
Screw Hole



PCB Federal Mark PAD

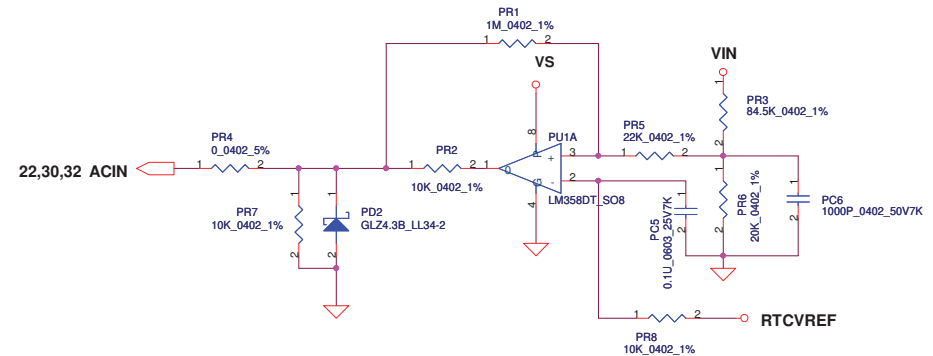
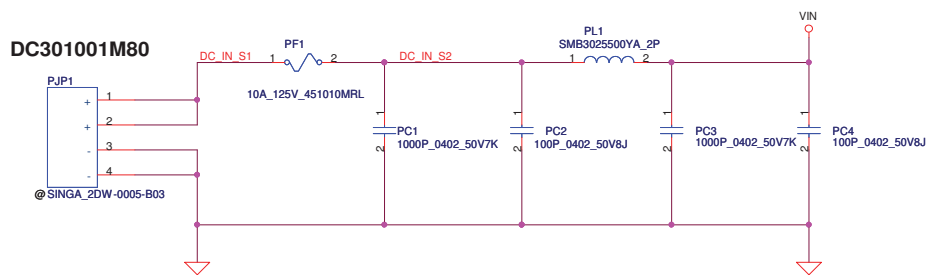


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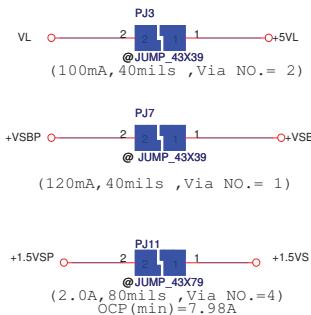
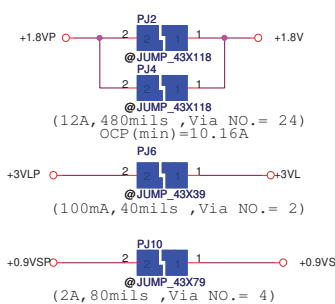
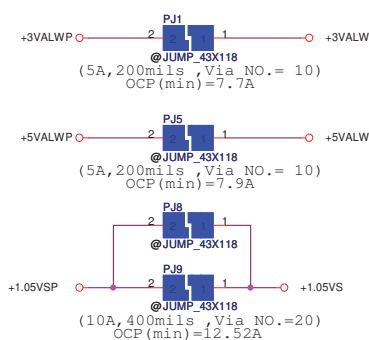
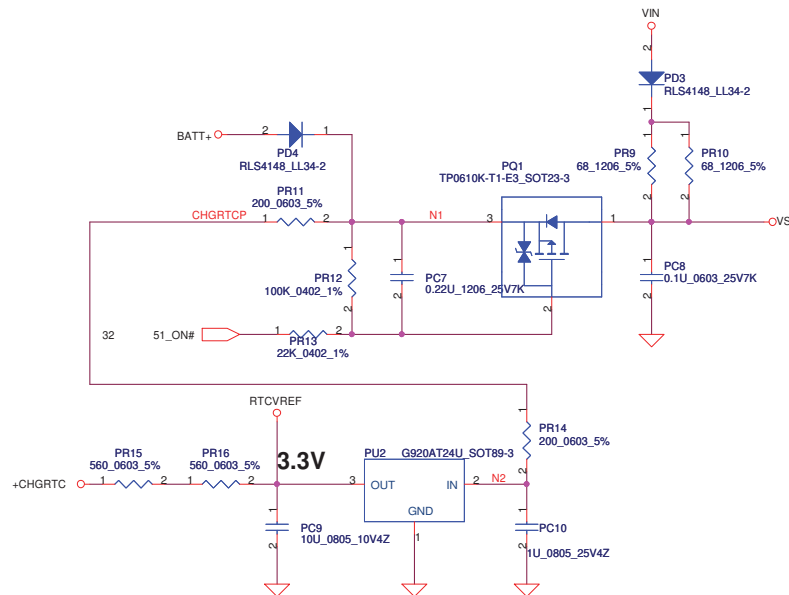
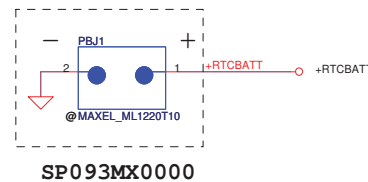
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Vin Detector

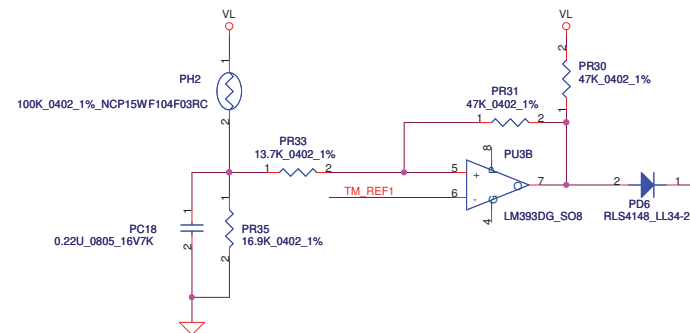
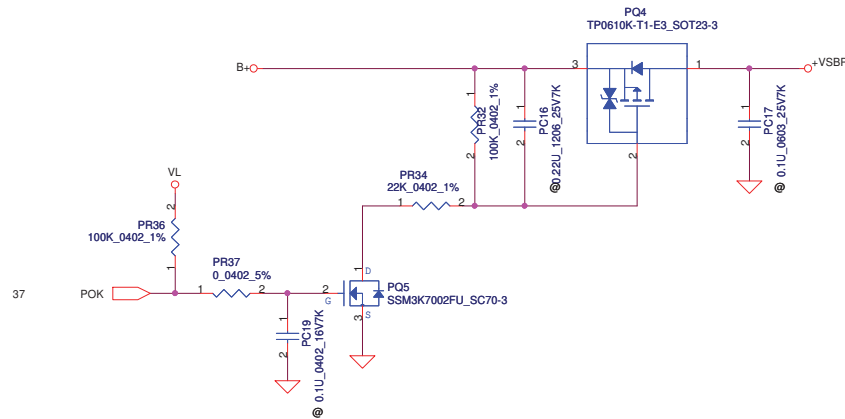
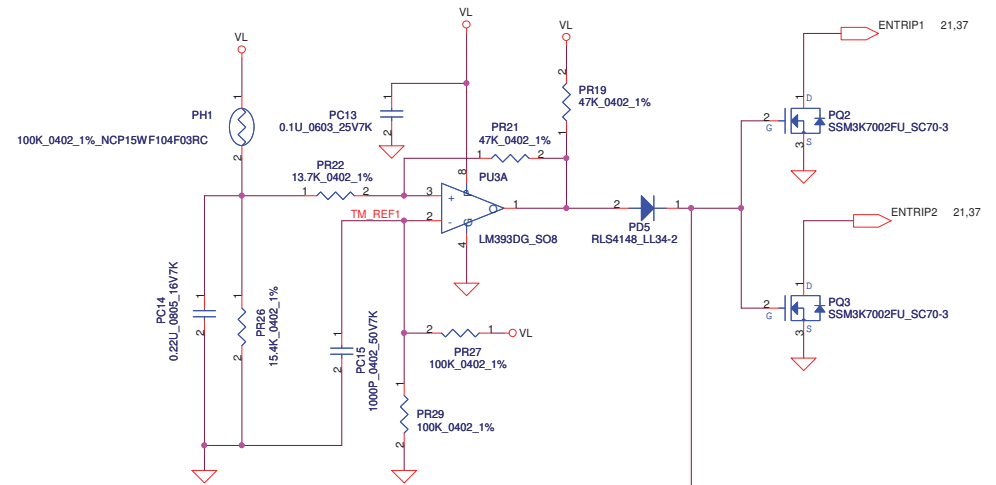
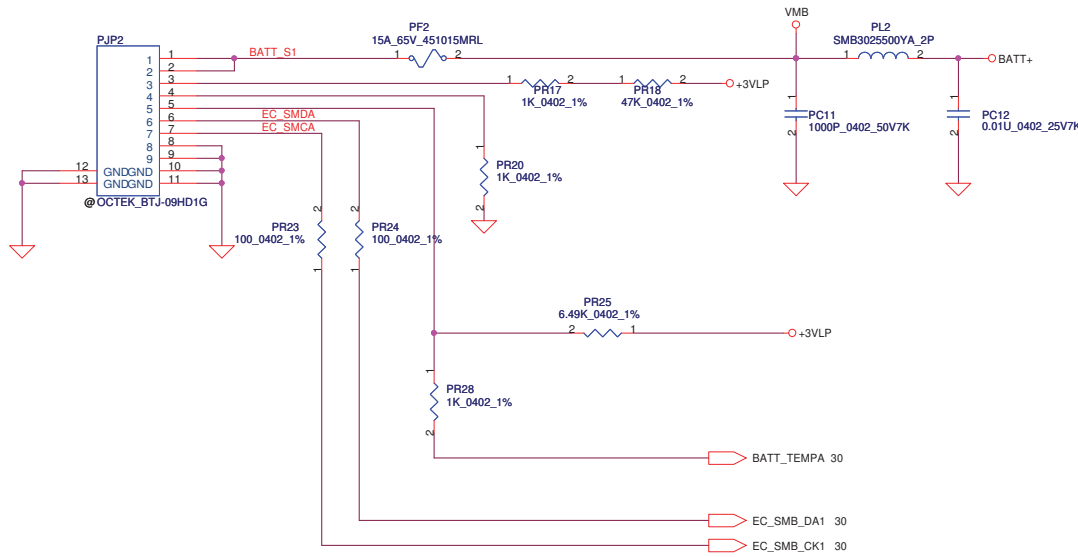
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

RTC Battery



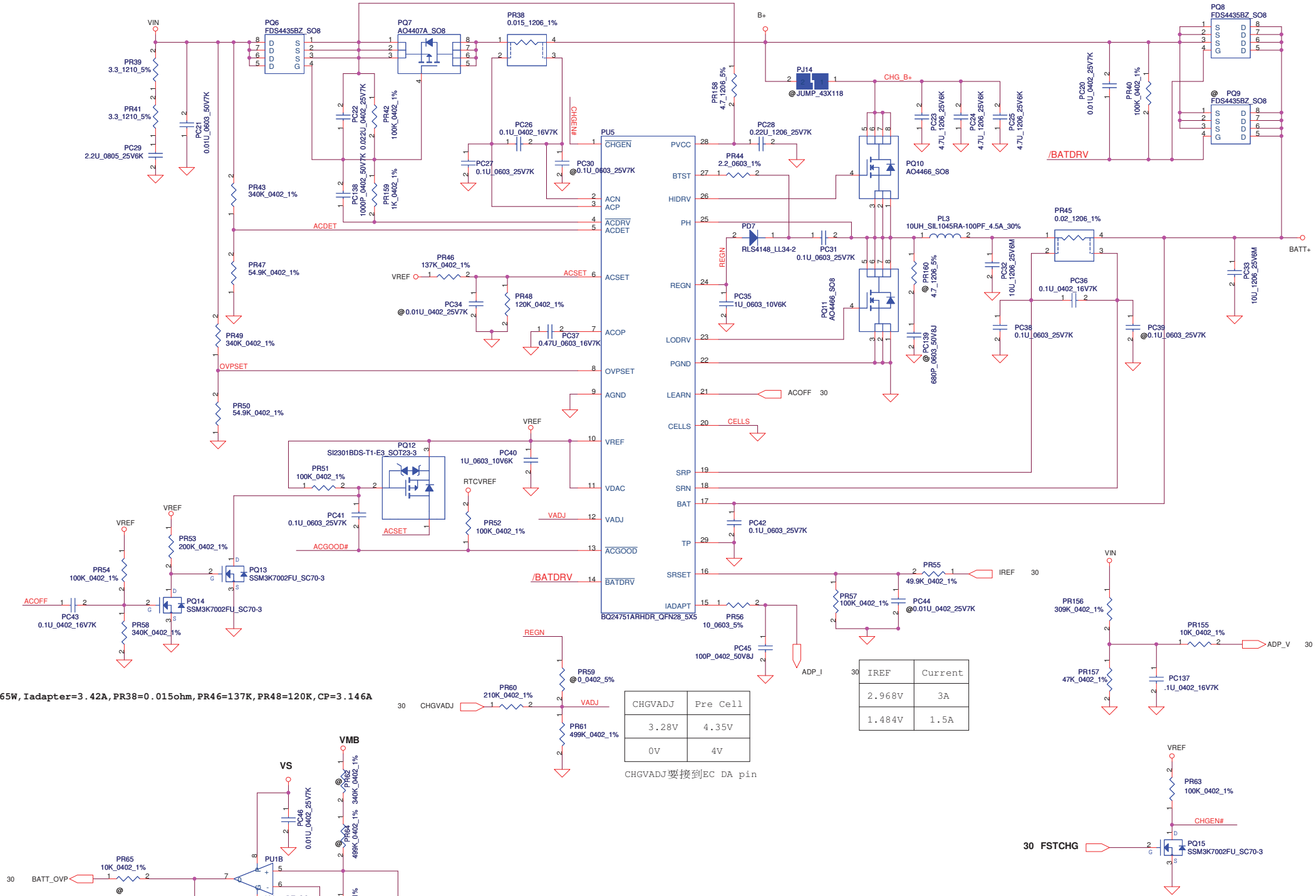
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/07/28	Deciphered Date	2010/07/28	Title	
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Size	Document Number	KTKAA		Rev	
Date: Monday, August 10, 2009	Sheet	34	of	41	1.0

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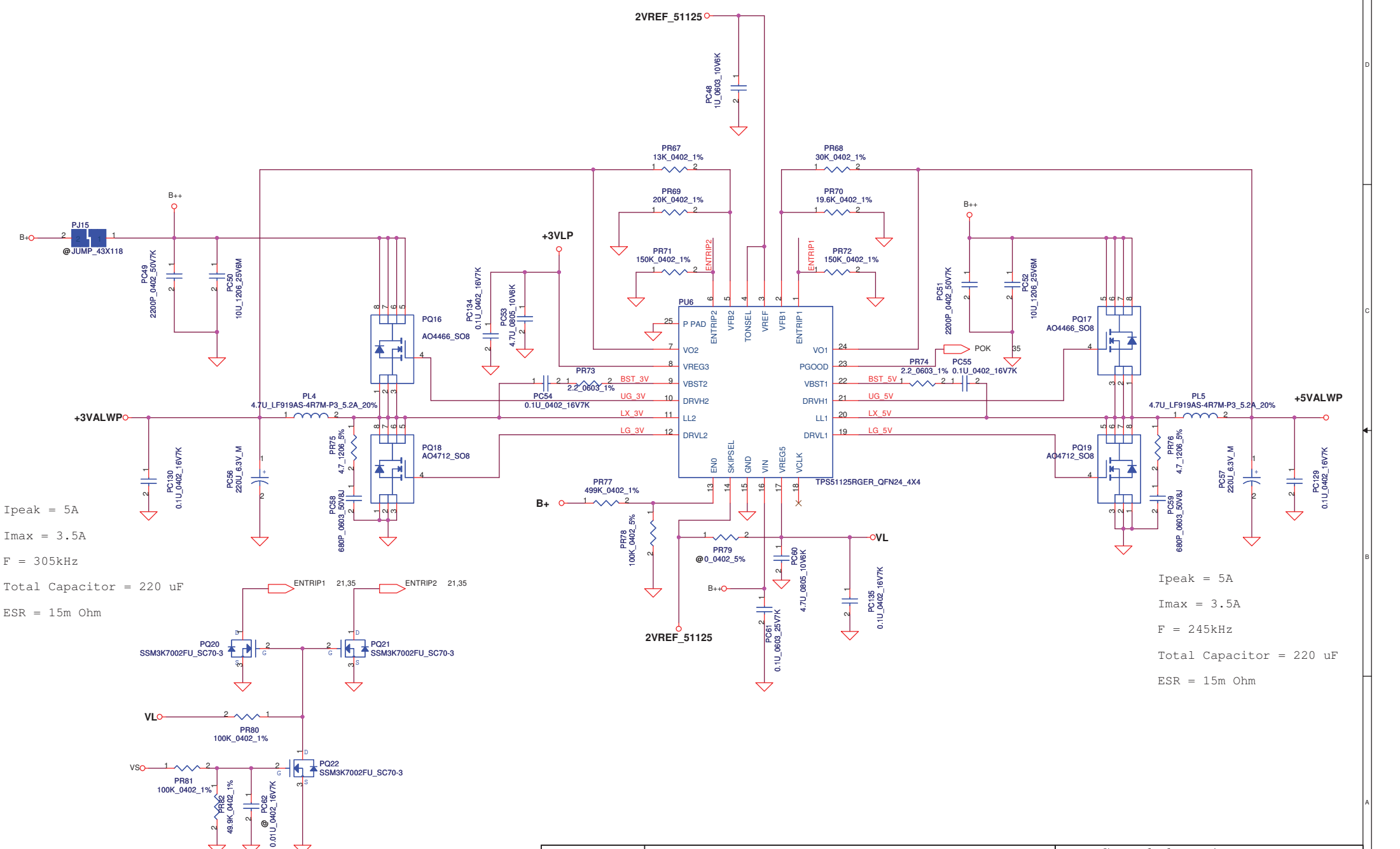
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Issued Date	2009/07/28	Deciphered Date	2010/07/28	Title	
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Size	Document Number	Rev			1.0
Date:	Monday, August 10, 2009	Sheet	35	of	41

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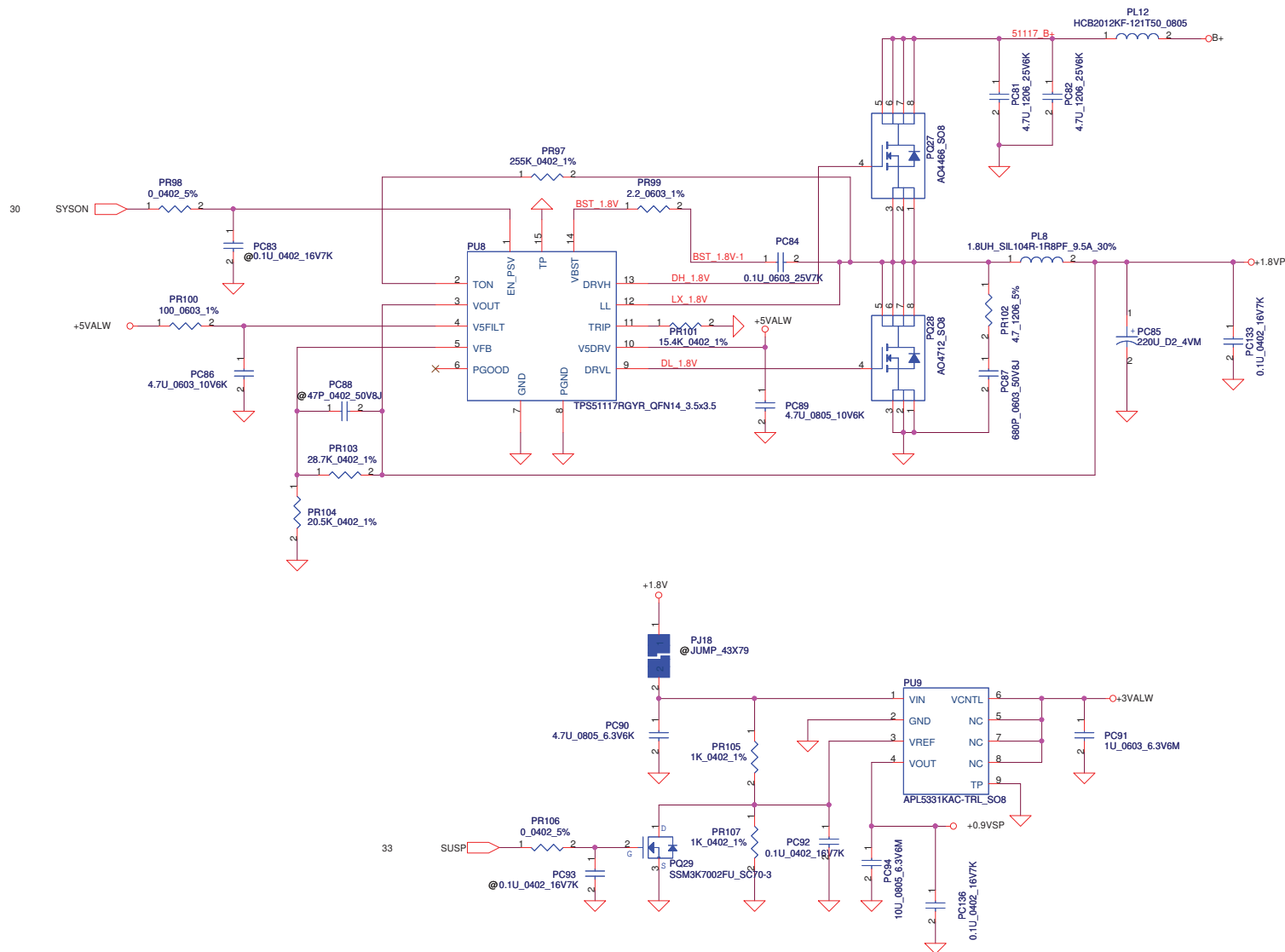
Ipeak = 5A
 Imax = 3.5A
 F = 305kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm

Ipeak = 5A
 Imax = 3.5A
 F = 245kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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										+5V/+3V	
										Size	Rev
										Custom	1.0
										Date	Monday, August 10, 2009
										Sheet	37 of 41

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Ipeak = 8A
 Imax = 5.6A
 F = 312kHz
 Total Capacitor = 440 uF
 ESR = 7.5m Ohm

Security Classification				Compal Secret Data			Compal Electronics, Inc.		
Issued Date				2009/07/28		Deciphered Date	2010/07/28		Title
									1.8V / 0.9V
							Size	Document Number	Rev
									1.0
							Date:	Thursday, August 06, 2009	Sheet 39 of 41

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PIR (Product Improve Record)

NBWAA LA-5821P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/06	18	Add R936 on BKOFF#; R937 on INVT_PWM	To prevent EC pin damage
2.	08/06	26	Add RL90, RL91, RL91 on +3V_LAN	For EMI's request
3.	08/06	18	Add C922, C923, C924 220pF on DAC_BRIG, INVT_PWM_R, BKOFF#_R	For EMI's request
4.	08/06	31	Delete R752, C787 on SPI_CLK; Add L912, C925 on SPI_CLK_L	For EMI's request
5.	08/06	28	Add LA11 on INT_MIC_L	For EMI's request
6.	08/06	28	Mount D61, DA3, DA6, DA7	For ESD's request
7.	08/06	32	Un-mount SW5, SW6	Power button, no need after pre-MP

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/07/28	Deciphered Date	2010/07/28	Title ISPD	
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					NBWAA LA5821P M/B
				Date	Monday, August 10, 2009
				Sheet	41 of 41
				Rev	1.0

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